HARDWARE DESIGN OF BASIC ISDN PSEUDO - TERNARY CODE TRANSCEIVER

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by

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C E R T I F I C A T E

It is certified that the work contained in the thesis entitled "Hardware design of basic ISDN pseudo-ternary code transceiver" by "Maj I S Chowdhary" has been carried out under our supervision and that this work has not been submitted elsewhere for a degree.

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ABSTRACT

The present state of development of communication technology is characterised by two main features; namely the digital transmission and processing, and integration of technologies and services. Multi-service terminals are designed to handle more than one kind of information. The ISDN allows voice, text, or data to be transmitted on the same circuit and provides effective integration of technologies and of services (by using multi-service terminals) for communications. The two types of access for the ISDN, Basic and Primary, ensure connectivity of a wide variety of terminal equipments that can possibly be used in the network.

Basic access is used for the interconnection of the terminals and switches. The signal that is transmitted on the line is a three level signal, and not a binary signal, which is suitably coded resulting in a pseudo-ternary code. We present outline of our effort to fabricate the pseudo-ternary transceiver in a MSI chip configuration. Reducing the chip configuration to flip-flop and gate levels, while implementing the hardware, has been accomplished. This would further enable the ISDN interface to be fabricated in PLA or FPGA configuration. In our work, apart from recovery of the original data from the three level signal, a robust and a general purpose timing and frame sync recovery scheme has been implemented.

A C K N O W L E D G E M E N T

I am deeply indebted to Dr V Sinha and Dr K R Srivathsan for their invaluable help and guidance. Their constant and careful guidance, instilled a motivation that helped me to carry through the most difficult phases of the work with unflagging enthusiasm.

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I.S. CHOWDHARY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER-1

INTRODUCTION

1.1 INTEGRATION

For over a century the primary communication workhorse has been the Telephone System. The system was designed for analog voice transmission. However, with the changing communication scenario it is proving inadequate for growing communication needs; such as data transmission, video, facsimile etc. Service dedicated networks have been conceived and implemented, to provide in a cost effective manner a limited range of services centered around the main service applications to which they are devoted. The fast growing demand for new communication services along with recent advantages, in technology create strong incentives for the development of an Integrated Services Digital Network (ISDN). The ISDN has primary goals of integrating voice and non-voice services. Efficient digital transmission and switching facilities to provide both types of services are, therefore, required. In view of the trend to use digital technology for different services (voice and non-vioce) for public and private networks, it is clear that such integration can only lead to economical advantages.

Obviously the fundamental motivation for integrating all services into common facilities arise from savings obtained by

sharing the transmission links. There are two aspects of sharing transmission links. First, the reduction in the total transmission capacity required to provide a given grade of service; when separate networks are used each network includes spare transmission capacity to accomodate traffic overloads and failures. When the networks are combined, so that various services share the transmission facility, on dynamic basis, spare capacity is shared by all traffic types and fewer total circuits are required. The amount of savings to be obtained by sharing circuits in dynamic manner is strongly dependent on the circuit utilization of the individual networks. If the circuits are lightly utilised, significant reduction in the total transmission capacity is possible. If, however,the transmission links of each network are heavily utilised, a combined operation may result in a marginal saving. The second, and usually more important reason for combining services, is the savings realised by using common maintenance, testing and repair procedures. ISDN will make it practical in an affordable fashion to integrate existing services and new technologies into a network that can handle telephone, data and other services. It will truely be a SUPERNETWORK providing universal, accessible flexible telephone and information services [1].

1.2 THE ARRIVAL OF ISDN [1]

The ISDN will be world wide public telecommunications

network that will deliver a variety of services. To control ISDN evolution and impact, massive effort at standardisation is underway. Although ISDN standards are still evolving, both technology and emerging implementation strategy is well understood. By standardising the interfaces to the ISDN, all ISDN compatible equipment (eg. telephones, computer terminals etc.) will be able to attach to the network anywhere in the world and connect to any other attached system. This can lead to extra-ordinary flexibiity. Some sample of trends that will be accelerated by ISDN are

a) Computers will be joining together instead of standing alone on a scale totally unheard of, as of now.

b) Communication will get further mobile by means of cellula radio, which will be developed a great deal with the advent of the ISDN.

c) The volume and richness of data will increase dramatically.

d) Promotion of national and global business activities will become easy and simplified.

e) Person-to-person interaction will increase considerably.

f) The fiber-optics along with ISDN will result in a quantum jump in the field of communication over terrestrial networks.

1.3 EVOLUTION OF ISDN

ISDN will not happen overnight. The transition from the

existing network to a comprehensive network will require a long period. The investment in the current telephone industry is so great that ISDN will have to be ushered in over a period of decades and it will have to coexist with the present system for many years before it would exist independently. We shall be well within the 21st century when eventually the existing transmission and switching network will be replaced by the integrated one. During the last two decades, architecture and standards for digital transmission network dedicated to voice and data have been established worldwide, such networks are called Integrated Digital Networks (IDN), where integrated refers to commonality of digital techniques used in transmission and switching systems.

Three main stages for evolving ISDN architecture are envisaged [4]:

a) An early ISDN architecture for voice and data capability. In the early stages the network would be implemented by integrating it with the present network system, i.e. hybrid switching systems (circuit and packet switching) would characterise the ISDN.

b) An advanced stage for an enhanced integrated capability also for voice and data. Only packetized voice and data switching technique would be used in this stage.

c) An ISDN architecture for broadband capability, i.e. upto several hundred megabits channel capacity would be available with the help of fibre optic transmission media.

1.4 TECHNOLOGY

The ISDN concept has emerged in the era where the advances in microelectronics, software production and digital technology has gained new heights. Significant contributions in the field of chip technology, namely the large scale integration (LSI) and very large scale integration (VLSI), in combination with OSI protocol architecture, has resulted in the availablity of the ISDN infrastructure in these latest chip technologies. User-network interfaces, too, are available in the said chip technologies, but no interface in the MSI chip technology is available, not considering the other forms of networks such as LAN's, WAN, or other up-coming compatible ISDN networks. The heirarchy in terms of complexity in technology are

a) MSI,

b) PLA's,

c) LSI and

d) VLSI.

1.5 2B + D - ISDN

Two accesses types in the ISDN scenario are the Primary Access and the Basic Access.

a) Primary Access - It is used for connecting switches to other switches or for connecting host computers to switches. Typical example would be interconnections of PABX's in a private

networks and interconnection of PABX to a private network exchange.

b) Basic Access - It is used for interconnections of terminals and switches. Switches could be public network exchages or PBX's in private networks. This access is intended to service single or multiple ISDN terminal installations (upto 8 terminals in multidrop mode). A signal of total bit rate of 192 kbps is transmitted in both directions (net bit rate available for traffic is 144 kbps). As individual subscriber one would be concerned with the Basic Access only. The binary data after being multiplexed with the control signals results in a 192 kbps bit stream. This bit stream is then suitably coded to give a three level signal which is transmitted on the line.

These are dealt with in detail in chapter 3 (refer to section 3.6). For convenience, as well as for better understanding of the waveforms transmitted on the line, 2B+D, i.e. Basic Access, transmitted bit stream implementation has been considered.

1.6 THESIS OUTLINE

The aim of the present work is to design and implement a Transceiver for Basic access interface with MSI chip configuration. In the technology of VLSI/LSI, the complete MSI chip configuration of the said interface Transceiver has been implemented by means of two or three IC's only. Indepth study of the waveforms at each stage of the work allows us understanding of

the physical layer of the system.

The thesis is organised on the guide lines of the 'Thesis Guide'. After introducing the ISDN and the thesis work in chapter one, in chapter two the ISDN concept, in general, is discussed. In chapter three user-network interfaces, with particular reference to basic access interface is presented. Chapter four deals with the hardware implementation, the results acheived and detailed documentation. The thesis is concluded in chapter five along with a few suggestions.

CHAPTER-2

ISDN - CONCEPT

We present the general ISDN concept, in brief, in this chapter.

2.1 CHARACTERISTICS

The main feature of the ISDN concept is the support of a wide range of voice and non-voice applications on the same network. ISDN means transmitting, at high speed over regular telephone lines, digitally encoded voice, data and other services multiplexed. An ISDN can be characterized by the following main features [2, 4]:

a) End-to-end digital connectivity.

b) Based on, essentially 64 kbps telephone channel.

c) Basic access, (2B+D), and Primary access, (24B+D or 30B+D) are to be provided on copper wire pairs of existing subscriber lines (B - 64 kbps; D - 16/64 kbps).

d) To each subscriber a single directory number is allocated, irrespective of the number and type of service (voice, text or data).

e) Universal user-network interface, defined for the ISDN allows different terminals to be connected by a standard communication socket.

ISDN provides a network transport capability for a variety of services (ranging from telemetry to broadband video applications) using a variety of digital comminication modes [4]. An ISDN is recognised by the service characterstics (protocol performance etc.) offered at its access interface rather than by its internal architecture, configuration or technology. The concept plays a key role in permitting user applications and network technologies to evolve separately. Essential to the ISDN concept is indeed the integration over access interfaces and loops. Hence the ISDN may be implemented in a variety of configurations according to the particular telecommunication environment from which it emerges, in terms of initial network status.

2.2 THE OSI REFERENCE MODEL [5]

One of the most important concepts in data communications is the Open Systems Interconnection (OSI) Reference Model. This model serves as a framework, within which communication standards are developed. It also serves as frame of reference for talking about data communications. Although ISDN recommendations represent a seperate effort from OSI and OSI - related standards, the ISDN protocols do fit within the OSI framework. The Purpose of this International Standard Reference Model of OSI, is to provide a common basis for the coordination of standard developments, for the purpose of systems interconnection. The OSI model proposes a

structured approach to protocol specification, based on seven-layer architecture. The key aspects to protocol layering are

a) Definition of homogenous function and procedures within each layer; which allows entities operating in the same layer to communicate correctly, and

b) The creation of boundaries between layers, so that each layer has direct interaction with two adjacent layers.

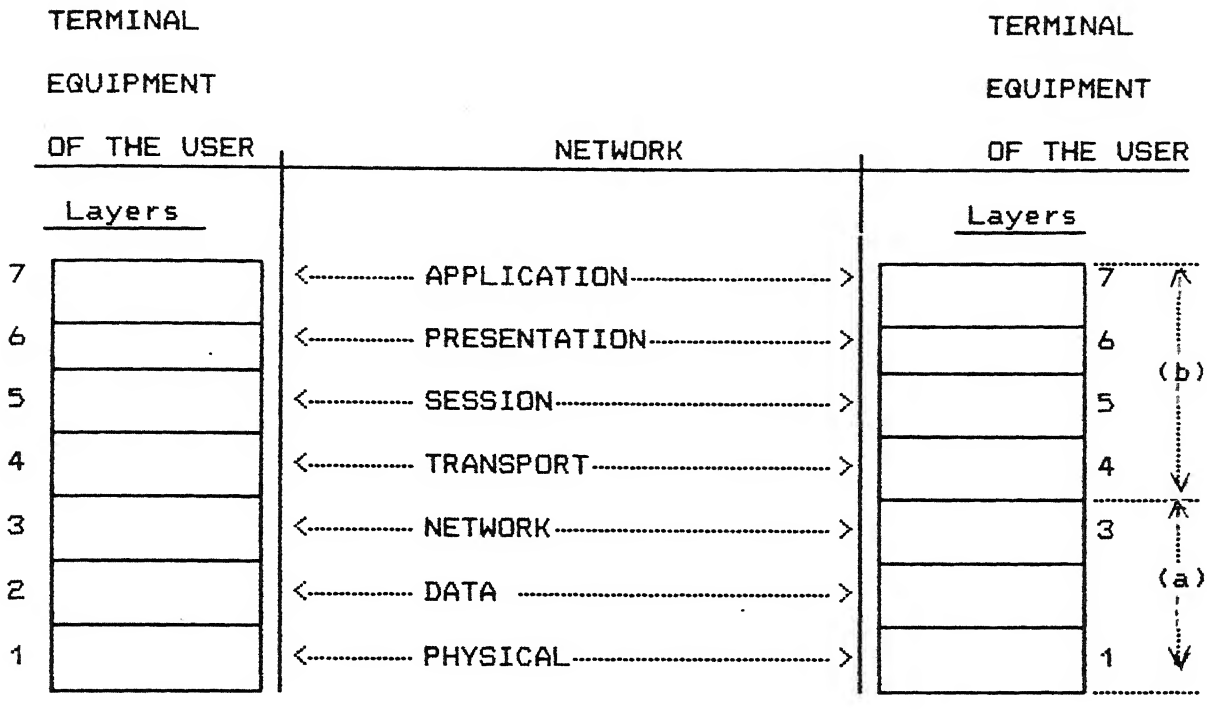
With a sequential number scheme from 1 through 7, each layer uses a set of services by the next lowered numbered layer and provides a larger set of services to the next higher numbered layer. Exceptions are layer 1 and 7 which offer services to and receive services, only from their adjacent layers, respectively. The protocols of layers 1 to 4 are transportation oriented i.e. they control both the access to the network (layer 1 to 3) and the transport of information through the network from user to user (end-to-end). These are shown schematically in Fig.2.1

2.2.1 THE SEVEN LAYER OSI REFERENCE MODEL.

The functions and protocols, classified according to the hierarchical structure of seven layers, of the OSI reference model, as shown in Fig.2.1, are dicussed briefly.

1) Physical layer is concerned with the transmission of bit stream over physical link; involves such parameters, as signal voltage swing and bit duration, deals with mechanical, electrical

and procedural characterstics to establish, maintain and deactivate the physical link.



a - Network access protocols,

b - End to end protocols.

Fig.2.1 :Structure of Protocols for communications between two terminals via a switched network.

a) Data link layer provides for the reliable transfer of data across the physical link; sends blocks of data (frames) with the necessary sychronization, error control and flow control.

a) Network layer provides upper layers from independence of data transmission, and switching technologies used to connect systems; responsible for establishing, maintaining and terminating

connections.

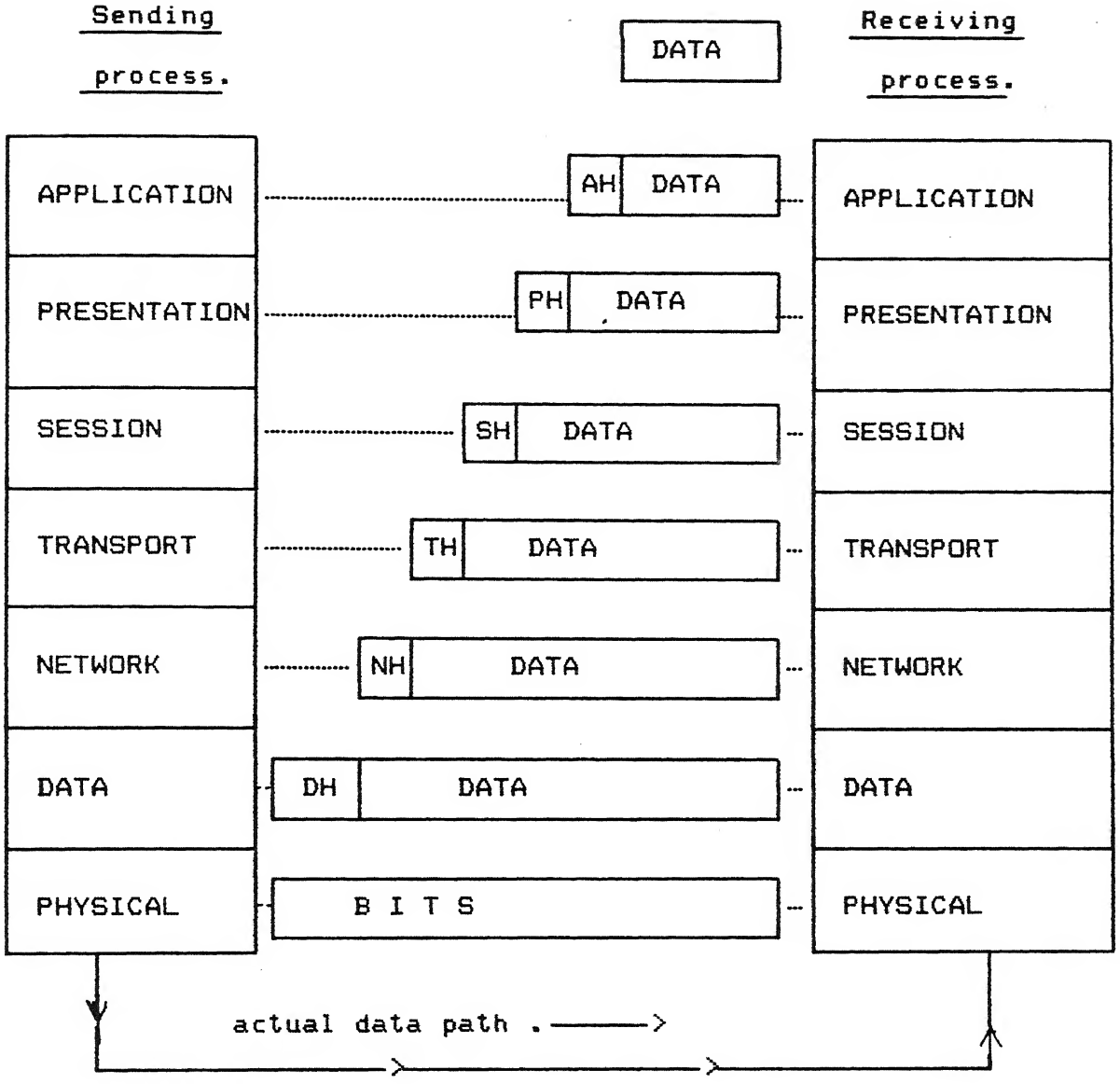
4) Transport layer provides reliable transparent data transfer between end points; provides end to end error recovery and flow control.

5) Session layer provides the control structure for communication between applications; establishes, manages and terminates connections between applications.

6) Presentation layer performs useful transformation on data to provide a standardized application interface and to provide common communication services. An example is encription. It is concerned with syntax and sematics of the information transmitted. It performs functions for presentation of information such as text and graphics character sets, format and structure of documents.

7) Application layer provides services to the users. It contains a number of protocols required for smooth functioning between different types of terminals. File transfer protocol and network management are two such examples. To this layer are also assigned the functions and protocols for controlling the applications (e.g. text transmission, text and data retrieval) and for editing and processing message contents for communication. Flow of information can be viewed schematically in Fig.2.2.

While protocols at layers 1, 2 and 3 are operated between user and network termination; protocols at layers 4 and above are operated end-to-end, across the network between end users. Layers 1 through 3 are chained and layers 4 through 7 are end-to-end.



H-Headers; Letters prefixing H denote the respective layers.

Fig.2.2 : Flow of information.

2.3 ISDN STANDARDS [1]

Although a number of standard organisations are involved in

various aspects of ISDN, the controlling body is the International Telegraph & Telephone Consultative Committee (CCITT). We shall see that the functions, interfaces and services embodied in ISDN, that are to be standardised, have a broad range. Because of complexity and because its success depends on the compatibility of providing true interconnectivity and interseperatability, standards are not only advantageous but also essential in the network. The development of ISDN is governed by a set of recommendations issued by CCITT, called the I-series Recommendations. The I-series Recommendations apply to the general concept and to the network capabilities of an ISDN, mainly in so far as they appear in the user-network interface and internetwork interfaces. These recommendations or standards were first issued in 1984 and a more complete set was issued in 1988. However, 1988 I-series Recommendations are not yet available hence the amendments/details incorporated in the recommendations have not been studied.

2.3.1 Structure of I-series Recommendations [6]

I-100 series - * General ISDN concept,
* Terminology, and
* General methods.

I.200 series - * Service aspects.

I.300 series - * Network aspects.

I.400 series - * User-network interface aspects.

I.500 series - * Internetwork interfaces.

I.600 series - * Maintenance principles.

The above structure shows the relationship of various I-series standards to each other. 1984 standards contained recommendations in series I-100 through I-600, some updates and extensions have occurred in these in the 1984-1988 period.

The I-100 series serves as a general introduction to the ISDN. The general structure of the ISDN Recommendations along with the glossary of terms peculiar to ISDN, overall description of ISDN and the expected evolution of the ISDN are also covered in this chapter.

The I-200 chapter is the most important part of the CCITT, ISDN Recommendations. The services to be provided to the users are specified. For CCITT a standardized service is characterised by:

a) complete, guranteed end-to-end compatibility,

b) standardized terminals including procedures,

c) standardized testing and maintenance procedures, and

d) charging and accountng rules.

I-300 series. The I-200 series focuses on the user, in terms of the service provided to the user, I-300 series focuses on the network, in terms of how the network goes about providing these services.

I-400 series deals with the interface between the user and the network. Three major topics addressed are:

a) Physical connections, the issue how the ISDN functions are configured into the equipment.

b) Transmission rates: the data rates and the combination of data rates to be offered to the user, and the transmission bit rates required for the signaling.

c) Protocol specifications: the protocols at the OSI layers 1 through 3 that specify the user-network interfaces.

2.4 TELECOMMUNICATION SERVICES [2]

Services supported by an ISDN, are the communication capabilities made available to the customers. An ISDN provides a set of network capabilities which are defined by standardised protocols and functions and enables various services to be offered to the customers. A service provision by the network provider, to a customer connected to an ISDN may cover the whole part of the means required to fully support the service. The service classification and description which follow are independent of different possible arrangements for ownership provision to the customer of the means required to support a service. Depending on the extent of standardization of communication functions and protocols, the services are divided into two groups:

a) Bearer services provide the means to convey information (speech, video, data) between users in real time and without alteration of the text of the message. These correspond to lower three layers of OSI model.

b) Teleservices combine the transportation function with the information processing function. They employ bearer services to transport data and in addition provide a set of high layer functions. The bearer services define requirements for and are provided by network functions. Teleservices include terminals as well as network capabilities. Examples are - telephony, teletex, videotex and message handling.

Both bearer and teleservices may be enhanced by supplimentary services .

Supplimentary services are the ones that may be used with one or more bearer or telesevices; they cannot be used alone. eg. call transfer, call forwarding, direct dailing etc. A supplimentary service modifies or supplements the basic telecommunication service, as mentioned it cannot be offered to a customer as a stand alone service. The same supplimentary service may be common to a number of services.

TELECOMMUNICATION-SERVICES

BEARER SERVICES		TELESERVICES	
BASIC BEARER SERVICES	BASIC BEARER SERVICES + +SUPPLIMENTARY SERVICES.	BASIC TELESERVICES	BASIC TELESERVICES + SUPPLIMENTARY SERVICES.

Depending upon different applications, too, services have

been identified into two categories

a) Distributive services - is communication between one transmitter and number of receivers. The information transfer is primarily one way. In this service it could be with or without individual users control; a stream of information from a central source to an unlimited number of receivers,in the network is transmitted. The service without individual control is called broadcast.

a) Interactive services - are services based on the exchange of information between two parties. It is further subdivided into three classes - conversational, messaging and retrieval.

Conversational services, in general provide the means for bidirectional dialog communication, with bidirectional end-to-end real time information transfer from user to user or user to host. Examples of conversational services are telephony, teletex, data transmission etc.

Messaging services offer user to user communication between individual users with store and forward, mailbox and/or message handling functions. Examples are mail services for audio information, text, data etc. These require centralised storage devices/units.

Retrieval services users are able to access information stored in information centres and are generally provided for public use. The information is sent to the user on demand. The information is retrieved on individual basis. Examples are retrieval service for data, text, graphics etc.

2.5 ISDN SYSTEM ARCHITECTURE [1]

We describe the ISDN Architecture, particularly the customers equipment and the interface between the user and network in this section through Fig.2.3. The key idea behind the ISDN is that of digital bit pipe, a conceptual pipe between the customer and the carrier, through which bits flow. The source is irrelevant, all that matters is that bits can flow in both directions. A digital bit pipe can and normally does support multiple independent channels by time division multiplexing of bit stream. The exact format of the bit stream and its multiplexing is carefully defined as part of user network interface.

Fig.2.3 is based on the CCITT Recommendation, I-310, and gives an architectural depiction of ISDN. The ISDN will support a completely new physical connecter for users, a digital subscriber loop, and variety of transmission services. The common physical interface provides a standardised means of attaching to the network. The same interface should be usable for a telephone, a computer terminal, a video terminal etc. Protocols are required to define the exchange of control information between users device and the network. Provisions must be made for high speed interfaces too, for example, a digital PBX or a LAN. The interface supports Primary and Basic accesses.

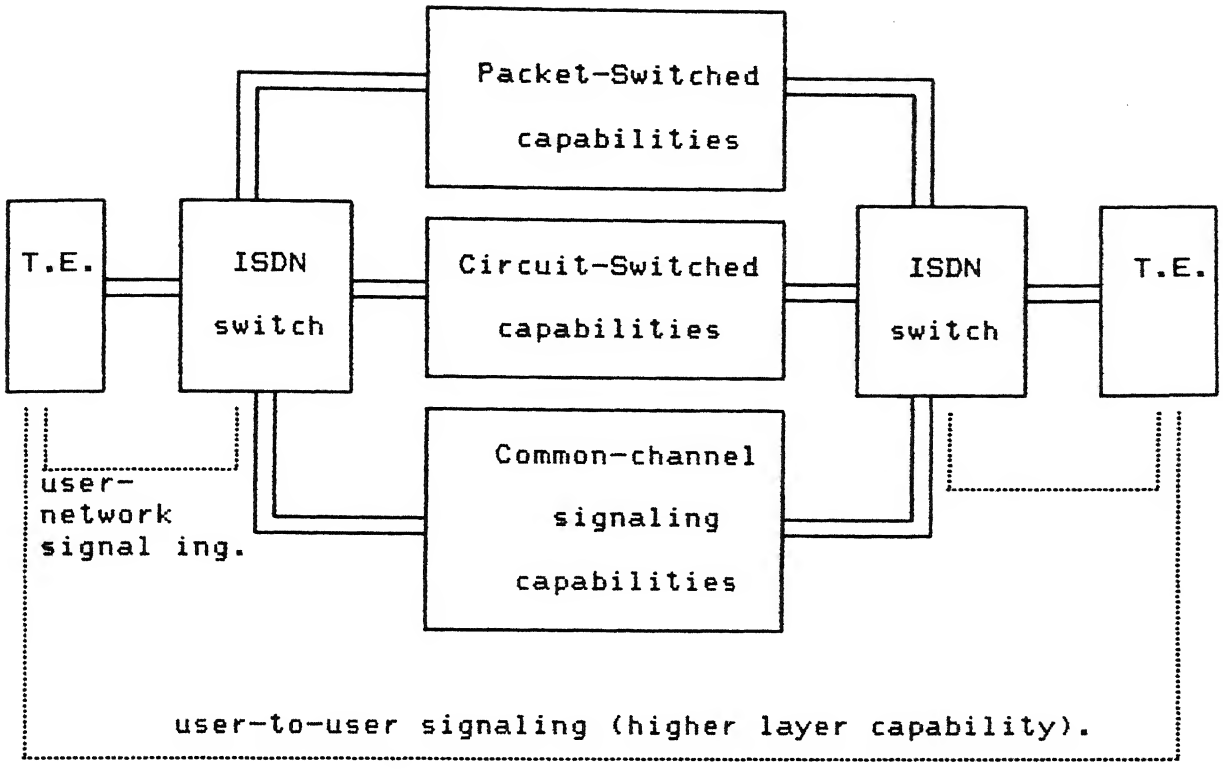


Fig.2.3: ISDN-Architecture

The subscriber loop provides the physical signal path from subscriber to the central office. The loop must support full duplex transmission for both basic and primary data rates. Initially most of the subscriber loop shall be on the twisted pair lines but as the network evolves and grows optical fibres will be used extensively. The ISDN central office connects numerous subscriber loops to the digital network. This provides access to variety of low layers (layer 1-3) transmission functions, including circuit-switching and packet-switching and dedicated facilities. In addition common channel signaling is used to

control network and provide call management; it will be accessible to the user. The signaling will allow user network dialog. The use of these control signal protocols for user to user dialog is a subject for further study. By and large the lower layer functions will be implemented within the ISDN.

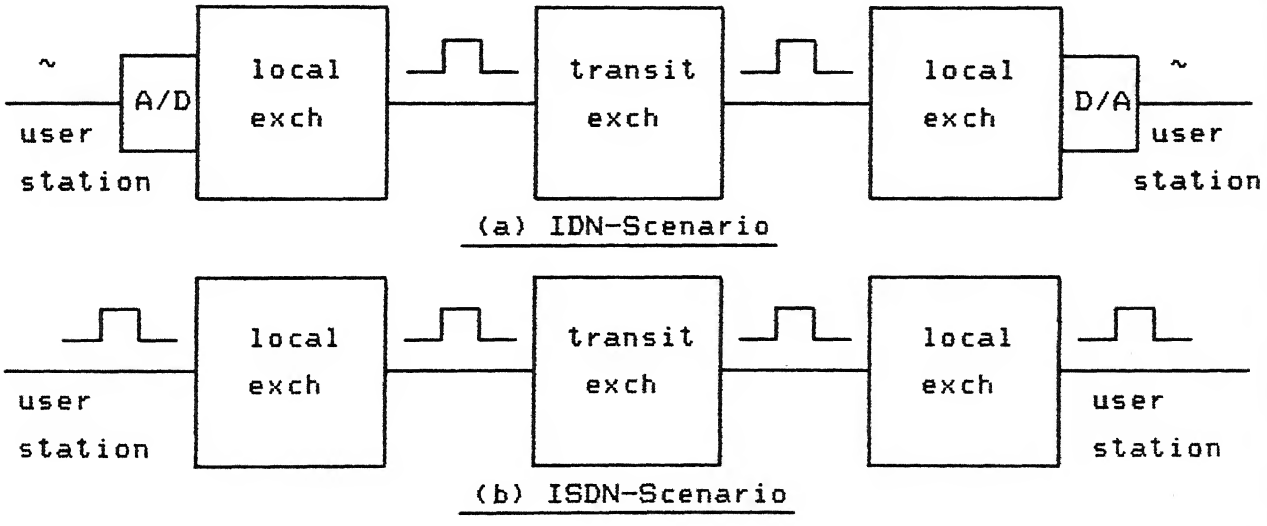
CHAPTER - 3

ISDN USER - NETWORK INTERFACES

In chapter 2 the ISDN concept was discussed in detail. In this chapter the user-network interface is dealt with extensively.

3.1 USER-NETWORK INTERFACE [2]

A traditional digital telephone network has digital transmission between two exchanges and analog transmission to/fro user equipments. Essential technical innovation of ISDN, apart from integration of services,is the digitization of the subscriber line as well (see Fig.3.1). Thus, integration of services and digitization at the user station are the main features due ISDN.



~ - Analog signal, ⎍ - Digital signal, A/D, D/A - Analog to Digital converter.

Fig.3.1: Network Concept

Fig.3.2 shows some examples of the ISDN user network interfaces. These are

a) Access by a single ISDN terminal,

b) Access by a multiple ISDN terminal,

c) Access by a multi-service PBX's or LAN's,

d) Access by a specialised storage and information processing.

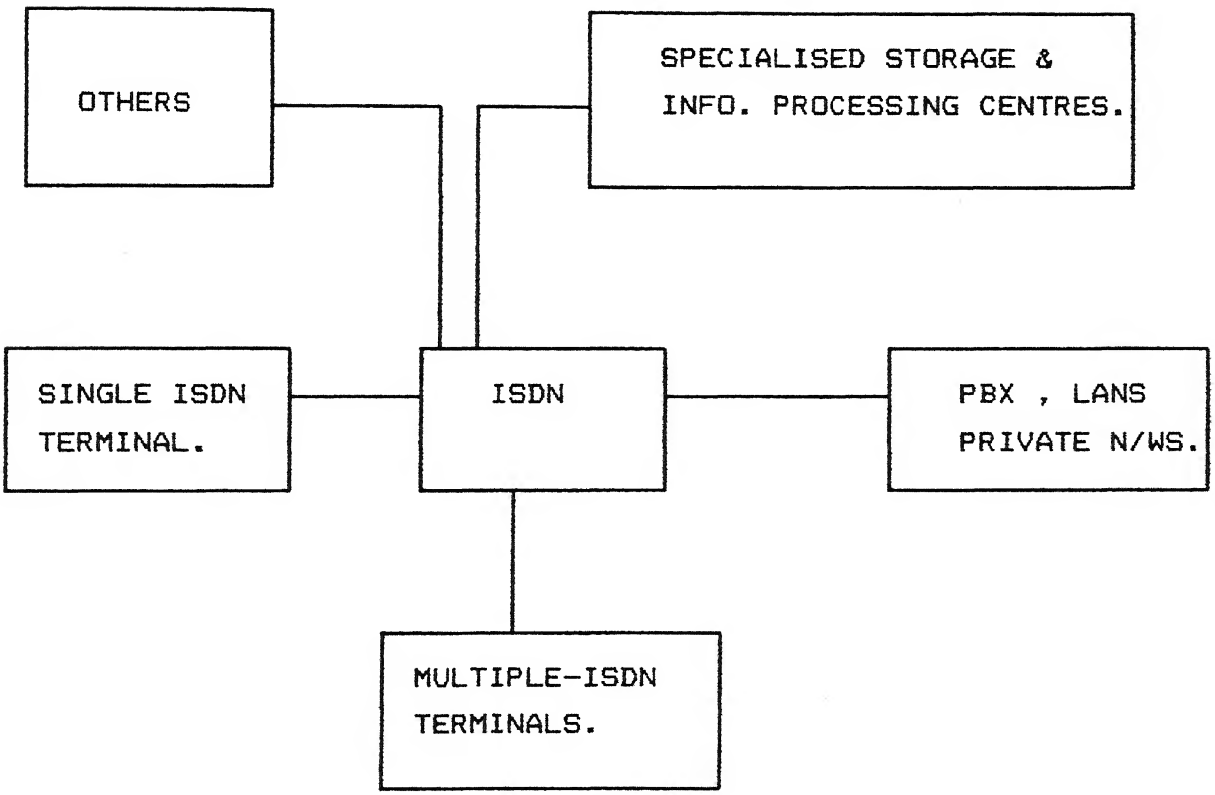


Fig.3.2: ISDN user-network interface examples.

In addition depending upon the particular national regulatory

arrangements, either ISDN user-network interfaces or inter-network interfaces may also be used for the access of

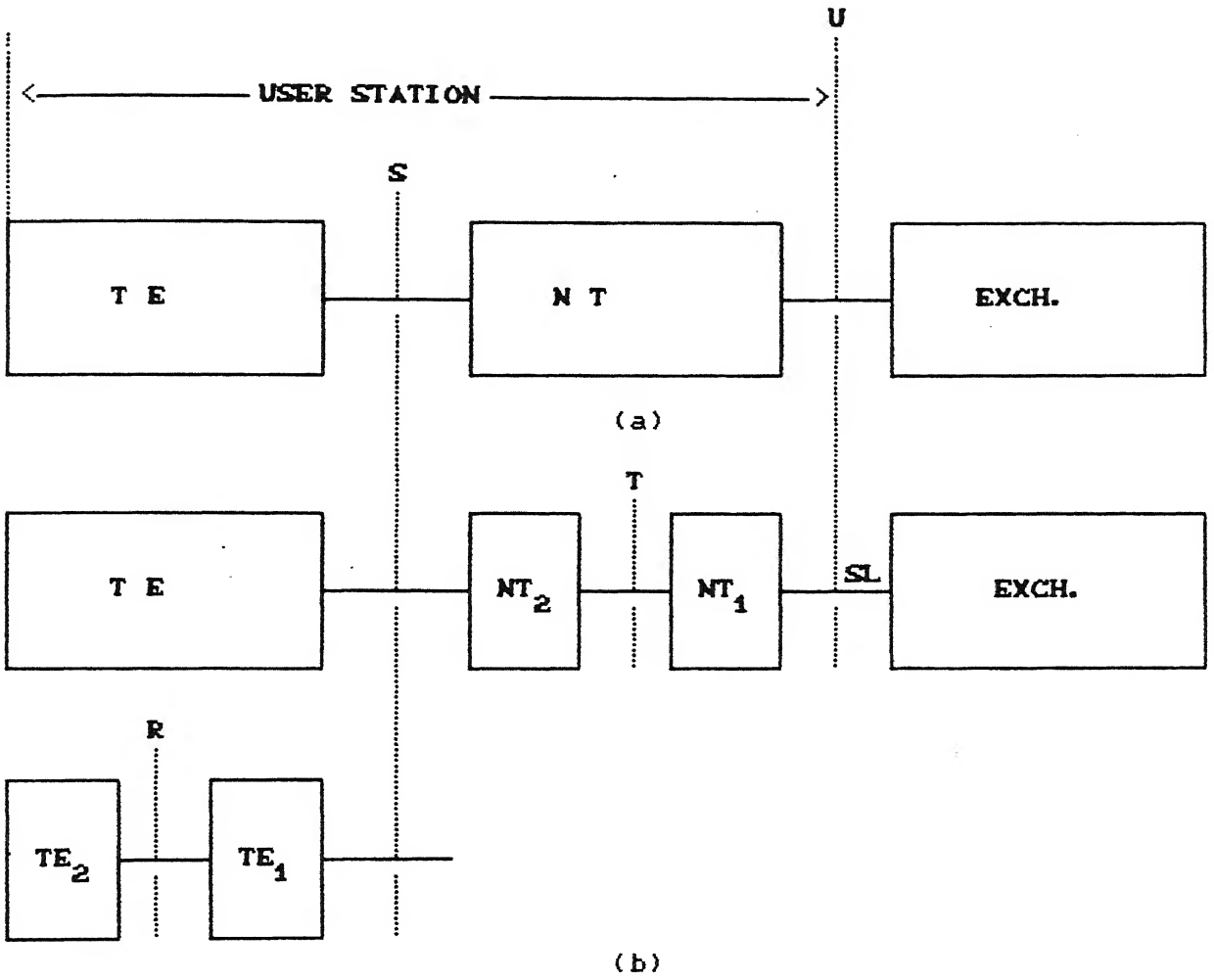
a) dedicated service networks and

b) other multiple service networks, including other ISDN'

3.2 CONFIGURATION OF THE USER-STATION [2]

From users perspective, an ISDN is completely described by the attributes that can be observed at an ISDN user-network interface; including physical, electromagnetic, protocol, service, capability, maintenance, operation and performance characteristics. User network interfaces should be designed to provide an appropriate balance between service capabilities and cost/tariffs, in order to meet service demand easily. The objective of ISDN is that a smallest set of compatible user-network interfaces can economically support a wide range of user applications, equipment and configurations.

To define the requirements for the ISDN user access, an understanding of the anticipated configuration of the neccessary standard interfaces is critical. The first step is to group functions that may exist on the users premises in ways that suggest actual physical configuration. Reference configurations for ISDN user-network interfaces define reference points and types of functions that can be provided between reference points. Functional groups are set of functions that may be needed in ISDN user access arrangement .They are certain finite arrangement of



SL - Subscriber line, NT, NT_1 & NT_2 - Network terminal,

TA - Terminal Adapter, TE, TE_1 & TE_2 - Terminal adapter,

Exch - Exchange, R, S, T & U - Refernce points.

Fig.3.3: Configuration of the user station.

finite equipment or a combination of equipments. Reference points are the conceptual points used to seperate functional groups. Fig.3.3 shows configuration of a user station.

NT: One or more Terminal Equipments (TE) are connected to the Network Termination (NT). The TE's could be of the same type or may be a combination of different types such as voice, and non-voice terminals. The NT physically connects the TE to the subscriber line and enables the latter to be used jointly by several terminals. NT is divided into two functional groups NT_1 and NT_2. NT_1 provides physical connection to the subscriber line. It is associated with the physical and electrical termination of the ISDN on the users premises. It may be controlled by ther ISDN provider and forms a boundary to the network. NT_1also performs line maintenance functions such as loop back testing and performance monitoring. NT_2 enables it to be used by several terminations i. e. joint use of network access by more than one TE's. NT_2 is an intelligent device and performs switching and concentration functions.

TE: The functional group TE can either be TE_1 i.e. specially designed for the ISDN and connected to the interface at reference points S or TE_2 with a conventional interface connected via TA. From the economic and the organisational standpoint the possiblity of connecting conventional terminals to the ISDN via a TA facilitates access to the ISDN for the user. TE_1 or TE_2+TA may be used interchangeably. Examples of TE_1 are digital telephones, integrated voice/data terminals and digital facsimile equipment. R.S.-232 is an example of TE_2; and thus would require TA to plug into an ISDN interface.

Reference Points between the functional groups have been defined :

a) Ref. Pt. T between network termination NT_1 & NT_2,

b) Ref. pt. S between NT & TE,

c) Ref. pt. R between TE_2 & TA, and

d) Ref. pt. U between NT & Exchange.

Reference point T (terminal) corresponds to a minimal ISDN network termination at the customer premises. It seperates the network providers unit from the users equipment. It was felt that there must be a decoupling of customer premises equipment from network technology and configuration. This would allow customers to preserve their investment, user equipment and software while the capabilities and performance characterstics evolve. Reference point S (systems) corresponds to the interface of individual ISDN terminal. It seperates user terminal equipment from network related communication functions. The S interface is a four wire connection, two wires are used for transmit and two for receive. Reference point R (rate) provides a non ISDN interface between user equipment that is not ISDN compatible and adaptor equipment. Reference point U (user) describes the full duplex data signal on the subscriber line.

3.3 INTERFACE STRUCTURES AND ACCESS CAPABILITIES [3]

The user network interface specified for the ISDN is based on the concept of the ISDN as a universal communication

network, intended to enable any person worldwide to communicate by any method- using voice, text, data, or picture simultaneously- a network to which it must be possible to connect both specialised and multifunction TE's. A users transmission capacity requirement depends on the type and number of communication services used at the same time and may vary considerably from user to user. In order to cover a variety of requirements without an excessively large number of interface variants, the number of access types defined has been kept to the minimum. The two access types currently specified are-

a) Basic Access and

b) Primary Access.

These are dealt in detail subsequently. The net transmission capacity differs by atleast an order of magnitude. The network may not make the full transmission capacity available at the interface.

3.4 CHANNEL TYPES [2]

The net transmission capacity available at the user-network interface is subdivided into:

a) Traffic Channels - B channel is the traffic channel having a bit rate of 64 kbps. It carries a variety of user information streams but does not carry signaling information. It could carry:

i) voice encoded at 64 kbps,

a) data info corresponding to bit rates less than or equal to 64 kbps,

a) voice encoded at bit rates lower than 64 kbps alone or combined with other digital information stream.

Traffic channels currently defined by CCITT are of three types, with different transmission capacities as listed in Table-3.1

Table-3.1: Traffic Channel Description

CHANNEL DESIGNATION	BIT RATE (KBPS)
B	64 (64*1)
H_0	384 (64*6)
H_{11}	1536 (64*24)
H_{12}	1920 (64*30)

An H channel is intended to carry a variety of user information streams. A distinguishing feature is that H channel does not carry signaling information for circuit switching. Information streams that are likely to be carried are

i) fast facsimile,

ii) video,

iii) high speed data and

iv) high quality audio or sound programme material.

b) Signaling Channel (D channel) - is primarily intended to carry signaling information for cicuit switching. D channel may

also be used to carry Packet Switched data. Depending upon the type of access the D channel has the bit rate of 16 or 64 kbps.

3.5 ACCESS TYPES [6]

Two access types, as mentioned before, are currently defined for reference points S and T ;

a) The Basic Access - a signal with total bit rate of 192 kbs is used in both directions, the net bit rate then available for traffic channels and the signaling channel is 144 kbs.

b) The Primary Access - a signal with a total bit rate of 2048 or 1544 kbs is used in both directions , the net bit rate of 1984 or 1536 kbps is available for traffic and signaling.

3.6 INTERFACE STRUCTURES [2]

Table 3.2 shows the interface structures specified for the abovementioned access types.

Table-3.2: Interface Structures

NET BIT RATES	BASIC ACCESS	PRIMARY ACCESS	
	144 KBPS	1984 KBPS	1536 KBPS
B-channel structures	$B+B+D_{16}$	$30B+D_{64}$ $30B^a$	$23B+D_{64}$ $24B^a$
H_0-channel structures	- -	$5H_0+D_{64}$ $5H_0^a$	$3H_0+D_{64}$ $4H_0^a$
H_1-channel structures	-	$H_{12}+D_{64}$ H_{12}^a	- H_{11}^a
Mixed structures	- -	$n.B+m.H_0+D_{64}$ $n.B+m.H_0^a$	$n.B+m.H_0+D_{64}$ $n.B+m.H_0^a$

D_{16}-16kbps D-channel, D_{64}-64kbps D-channel,

a -The associated signaling channel is routed through different access.

3.6.1 BASIC INTERFACE STRUCTURE

In case of basic access there is only one interface structure, composed of two B-channels (64 kbps each) and one D-channel (16 kbps) for signaling; 2B + D. The B-channel may be used independently i.e. different services can be used independently at the same time. ISDN user - network physical interface, one or both B channels however maynot be supported

by the network. There are three reference configurations for specifying the characteristics for the Basic Access (see Fig.3.4)

a) The point to point configuration,

b) The passive bus and

c) The extended bus.

The passive bus, also called the Multi-Drop feature, allows connection upto eight devices to each single ISDN line, instead of having only one piece of equipment plugged into the ISDN phone line.

3.6.2 PRIMARY RATE INTERFACE STRUCTURE

These structures correspond to the primary rates of 1544 kbps and 2048 kbps. It is composed of number of B-channels and one D-channel, the bit rate of D-channel being 64 kbps.

At 1544 kbps primary rate the interface structure is 23B + D.

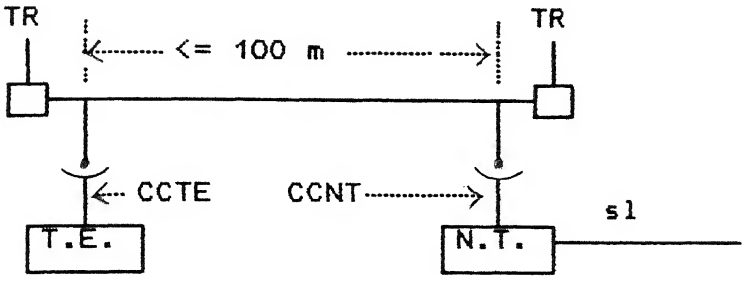
At 2048 kbps primary rate the interface structure is 30B + D.

With the primary rate B - channel interface structures, the designated number of B - channels is always at the ISDN user-network physical interface, and one or more B-channels maynot be supported by the network.

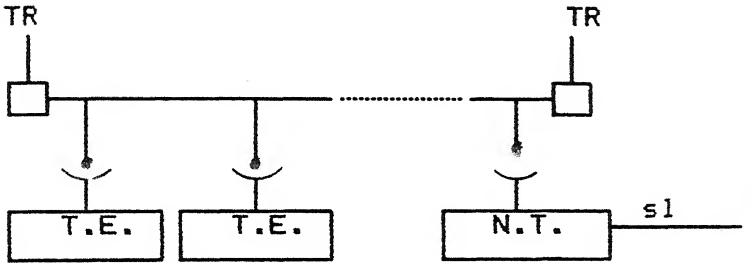
3.7 BASIC USER - NETWORK INTERFACE [2]

In the following, it is assumed that NT will indicate network terminating aspects of NT_1 and NT_2, and TE will be used to

indicate terminal aspects of TE_1 or TA and TE_2, unless otherwise

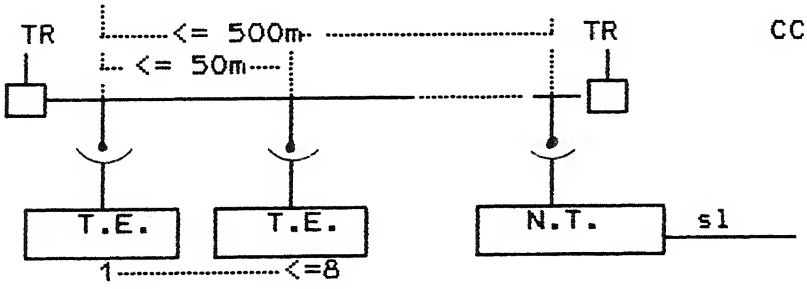


(a) Point to point configuration.



(b) Short passive bus.

sl - subscriber line
TR - terminating resistor
CCNT - connecting cord for N.T.
CCTE - connecting cord for T.E. .



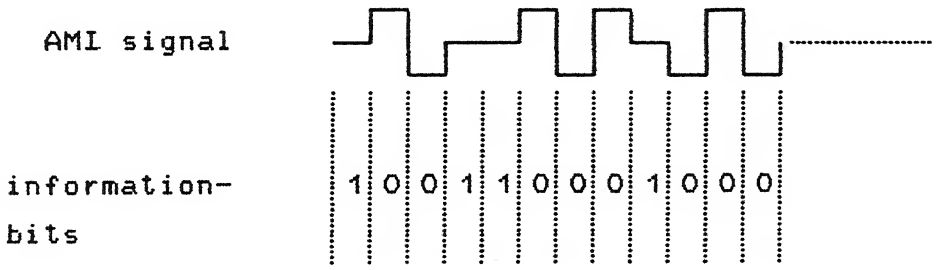
(c) Extended passive bus.

Fig.3.4: Reference configurations for specifying the characteristics for the basic access.

indicated (also ref to Fig.3.3). Two wire pairs are used at the

interface and these are for transmission, one pair for each direction. The NT can power the terminal equipments via a additional third wire pair. All the component signals, i.e. the D-channel signals, B-channel signals and the control signals, are combined by time division multiplexing. The multiplexed signal is then transmitted on a wire pair, in each direction. The transmission code used is the Alternate Mark Inversion (AMI) code, with 100% pulse width. Unlike the conventional AMI code, a zero is transmitted as a mark (pulse) and one as a space (no pulse) (Fig.3.5).

As mentioned above all the control signals along with information signals, in both the transmission directions are time division multiplexed, to form a 48 bit frame transmitted 4000 times per second. This corresponds to a total bit rate of 192 kbps



one : no pulse (space)

two : pulse (successive pulses have opposite polarity).

Fig.3.5:Transmission code for the Basic Access : AMI code with 100% pulse width,

(Fig.3.6). Rapid frame alignment is provided, by using double AMI code violation, and this is detected no later than the 14^{th} bit in the frame. The frame structures are different for each direction of transmission.

3.7.1 FRAME STRUCTURE

Terminal to network frame consists of the following group of bits, each individual group is balanced by its last bit (L-bit):

Bit position	Group
1,2	F -Framing signal with balance bit,
3-11	B_1-channel with balance bit (1^{st} octet),
12,13	D -channel with balance bit,
14,15	F_A-Auxillary framing bit with balace bit,
16-24	B_2-channel with balance bit (1^{st} octet),
25,26	D -channel with balance bit,
27-35	B_1-channel with balance bit (2^{nd} octet),
36,37	D -channel with balance bit,
38-46	B_2-channel with balance bit (2^{nd} octet),
47,48	D -channel with balance bit.

Network to terminal frames contain an echo channel (D-channel echo bit) used to retransmit the D-bits received from the terminals. D-echo control is used for D-channel access control. The last bit of the frame (L - bit) is used for balancing each

complete frame.

Bit position	Group
1,2	F -Framing signal with balance bit,
3-10	B_1 -channel bit (1^{st} octet),
11	E - D echo channel bit,
12	D - channel bit,
13	A - bit used for activation,
14	F_A - auxillary framing bit,
15	N - bit , coded as $\overline{F_A}$,
16-23	B_2 - channel bit (1^{st} octet),
25	D - channel bit,
26	S_1 - reserved for future standardisation,
27-34	B_1 - channel bit (2^{nd} octet),
35	E - D channel echo bit,
36	D - channel bit,
37	S_2 - reserved for future standardisation,
38-45	B_2 -channel bit (2^{nd} octet),
46	E - D channel echo bit,
47	D - channel bit,
48	L - frame balance bit.

For both directions of transmission, pseudo-ternary coding is used with 100% pulse width as shown in Fig.3.5. Coding is performed in such a way that binary one is transmitted by no line signal, whereas a binary zero is represented by a positive and

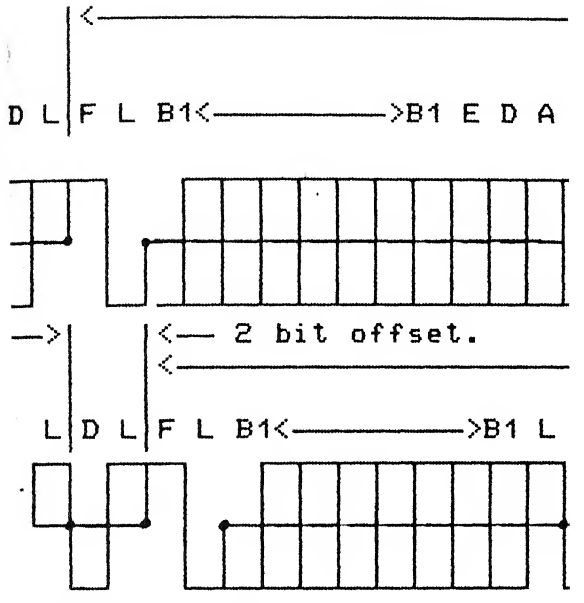
negative pulse, alternately. The first binary zero following the framing balance bit, has the same polarity as the frame balance bit. Subsequent binary zeroes must alternate, in polarity. The balance bit is binary zero, if the number of binary zeroes following the previous balance bit is odd; and balance bit is binary one if the number of binary zeroes following the previous balance bit is even.

NT shall derive its timing from the network clock. The TE shall synchronise its timing (bit, octet , frame) from the signal received from the NT and use this derived timing to synchronize its transmitted signal. The first bit of each frame transmitted from a TE towards the NT shall be delayed by two bit period, with respect to the first bit of the frame received from the NT, Fig.3.6 also illustrates the relative bit positions for both the transmitted and received frames.

D-echo channel - The NT on receipt of the D-channel bit from TE or TE's shall reflect the binary value in the next available D-echo channel bit position, towards the TE. Deactivation funtion is specified in order to permit TE and NT equipment to be placed in low power consumption mode, when no calls are in progress. Activation further allows TE or NT equipment to be restored back to its normal operating power mode.

Frame alignment: The first bit of each frame is the frame bit, F, and is a binary zero. The frame alignment procedure makes use of the fact that the framing bit is represented by a pulse having same polarity as the preceding pulse (AMI violation), this

ensures rapid reframing. To gurantee secure framing, the auxilary framing bit F_A and N in the direction NT to TE or F_A with associated balance bit, L, in direction TE to NT are introduced. This ensures that there is always an AMI violation at 14^{th} bit or less from the framing bit, F, due to F_A being zero bit (TE to NT or NT to TE). The coding rule for the auxillary framing bit pair F_A and N, in the direction NT to TE is such that N is binary opposite of F_A ($N = \overline{F_A}$). The F_A and L bits in the direction of TE to NT are always coded such that the binary values of F_A & L are equal.



- Framing bit,
- DC balancing bit,
- D channel bit,
- D channel echo bit,
- Auxillary channel bit (=0)

)TE-Dots demarcate the points

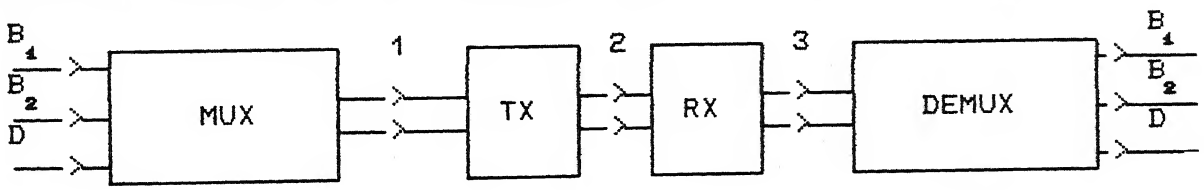
CHAPTER - 4

HARDWARE-DESIGN OF BASIC ISDN PSEUDO-TERNARY CODE TRANSCEIVER

In chapter-3 the user-network interfaces, alongwith the Pseudo-Ternary bit stream were discussed in detail. In this chapter the hardware implementation of the system is given.

4.1 THE TRANSCEIVER

Design of a conventional transceiver has been kept in mind while designing the Pseudo-Ternary code Transceiver. The three level bit stream, as shown in Fig.3.6, is obtained with the help of MSI chips at the transmitter. At the receiving end the original data, along with the clock and the frame sync signal are recovered from the three level bit stream by using the MSI chips. The block diagram of the designed system is given in Fig.4.1.



B_1, B_2 - Voice or data at bit rate 64 kbps,
D - Signaling at bit rate 16 kbps,
1 & 3 - Binary multiplexed bit stream at bit rate of 192 kbps,
2 - Pseudo ternary bit stream at bit rate of 192 kbps.

Fig.4.1: Block diagram of the transceiver

The design of the entire system is modular. The discussion regarding the design is divided into the following blocks:

a) Data source/Frame simulator.

b) Transmitter-

i) Multiplexing scheme,

ii) Insertion of the various bits, such as framing, balance etc.

iii) Generation and transmission of the Psuedo-Ternary code.

c) Receiver-

i) Data recovery,

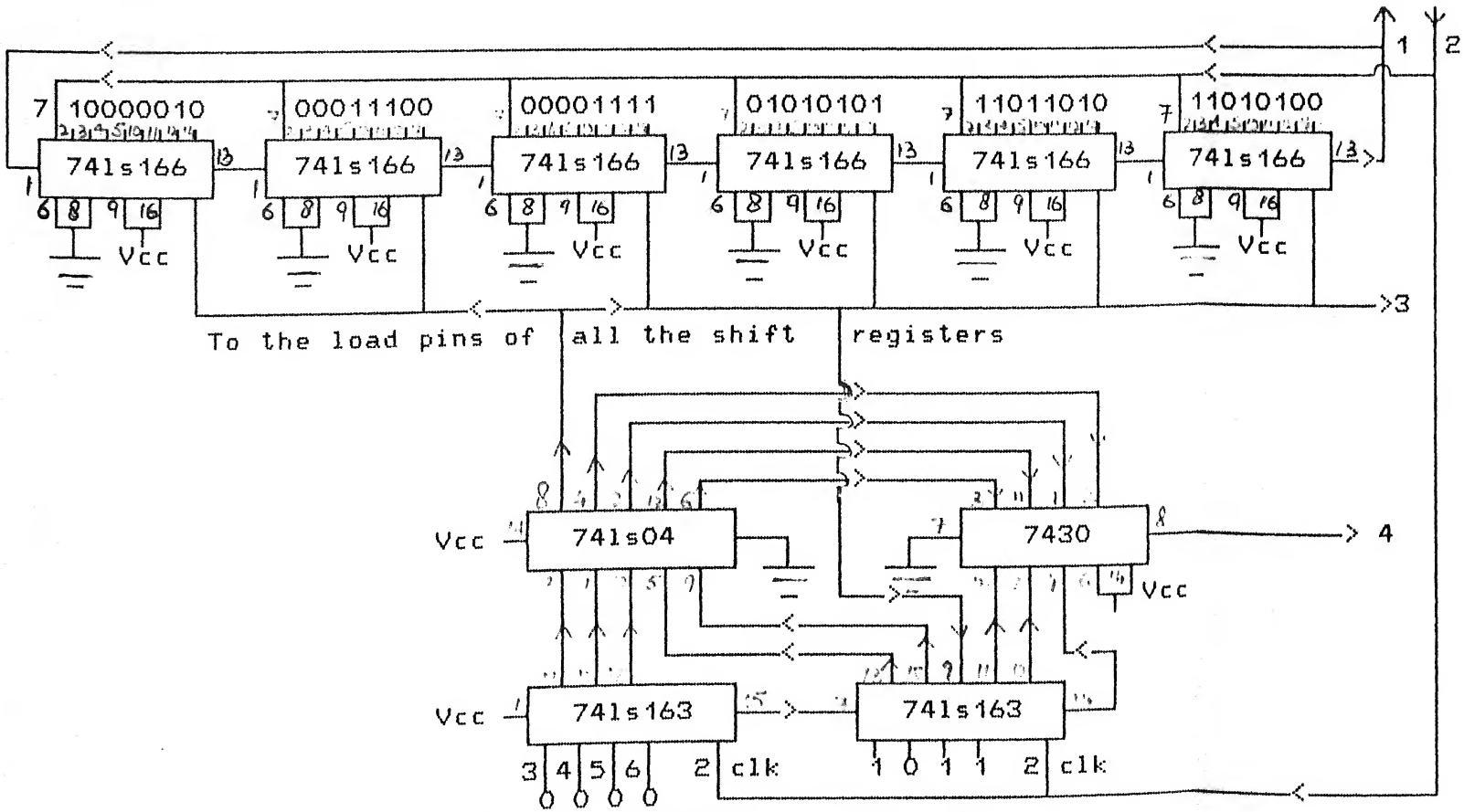
ii) Clock recovery,

iii) Frame sync recovery,and

iv) Demultiplexing scheme.

4.2 DATA-SOURCE (FRAME-SIMULATOR)

At present no ISDN compatible data source with appropriate fields is available. The said transceiver has been designed and fabricated on wire wrap. In order to test the transmitter and receiver, a Frame Simulator/Data Source has been implemented on bread-board. Referring to Fig-4.2, a multiplexed binary bit stream consisting of B_1 data stream, B_2 data stream and D signaling bit alongwith the other additional bits, as described in section-3.7, are made available at the output of the Data Source.



1 - Data output at output rate 192 kbps,
2 - clock input 192 kHz,
3 - frame sync signal (1/48 pulse),
4 - 2/46 pulse.

Vcc - 5V,
Pins not used are not shown,

Fig.4.2: Functional Diagram Data Source

The Data Source output is a binary bit stream of 48 bits, and this corresponds to number of bits in one frame. Six shift registers, parallel-input-serial-output, 74LS166, are used in series. Serial output of one is connected to the serial input of the next one, and all of them are clocked at the clock rate of 192kHz; thereby enabling the output data rate to be 192 kbps. Random data, corresponding to B_1, B_2 and D, are chosen but the balance bits are appropriate such that they conform to the CCITT standards. The other bits, too, such as F, F_A, N, A etc. are also chosen to meet the CCITT standards. These bits are made available at the parallel input ports of the shift registers, 74LS166.

Two binary counters, 74LS163, in series clocked at a clock rate of 192 kHz, ensure that a divide by 48 count is made available i. e. a pulse is available once every 48 clock cycles. The counters are used in an up-count mode. The binary value loaded at the parallel inputs of the counters is 47 short of the 2^9-1 (255) i.e. 208 (11010000). The ripple carry output (RCO) of the 1^{st} counter is fed to the ENP/ENT input of the 2^{nd} counter. The RCO of the 2^{nd} binary counter gives a pulse once every 48 clocks. This pulse is then used to load the parallel data in the six shift registers and the binary value in the binary counters. The pulse is also seen on the oscilloscope as start of a frame. We shall from now on call this pulse as the Frame Sync Pulse.

In the transmitter segregation is to be done between the first two bits and rest of the 46 bits of the frame, the requirment has been explained in detail in section 3.7.1. To

achieve this the Q_B, Q_C,& Q_D outputs of the first binary counter and Q_B of the second binary counter are inverted and fed alongwith Q_A, Q_C & Q_D of the second binary counter to an eight input nand gate, 7430, and the output is then again inverted to give a pulse that would be high for 1st two clocks and low for the rest of the 46 clocks, let us call this 2/46 pulse.

The outputs available at the Data source/Frame simulator are

a) Data, at the rate of 192 kbps,

b) Frame sync. pulse and

c) 2/46 pulse.

whereas the only input to the Data Source is a 192 kHz clock.

4.3 TRANSMITTER

The three outputs of the Data Source are available at the inputs of the transmitter, as mentioned in the previous section. Fig.4.3 refers to the block diagram of the transmitter and the Fig.4.4 gives the block schematic diagram of the transmitter.

2/46 pulse is fed to the D input of the D-flip flop (D_{1A}), it is also given a clock of 192 khz, the Q output is high for first two clocks and low for the rest of the 46 clocks. This output is ANDED with the clock and is fed to the two clocks of another D-flip flop (D_{2A} and D_{2B}), to whose D inputs inverted data is fed. The two Q outputs of the D-flip flop are then ORed using IC 7432.

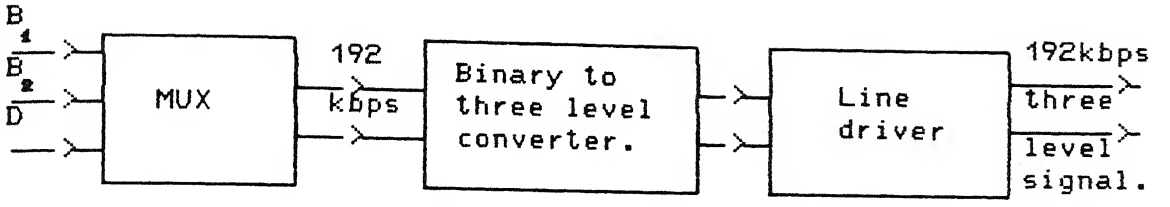


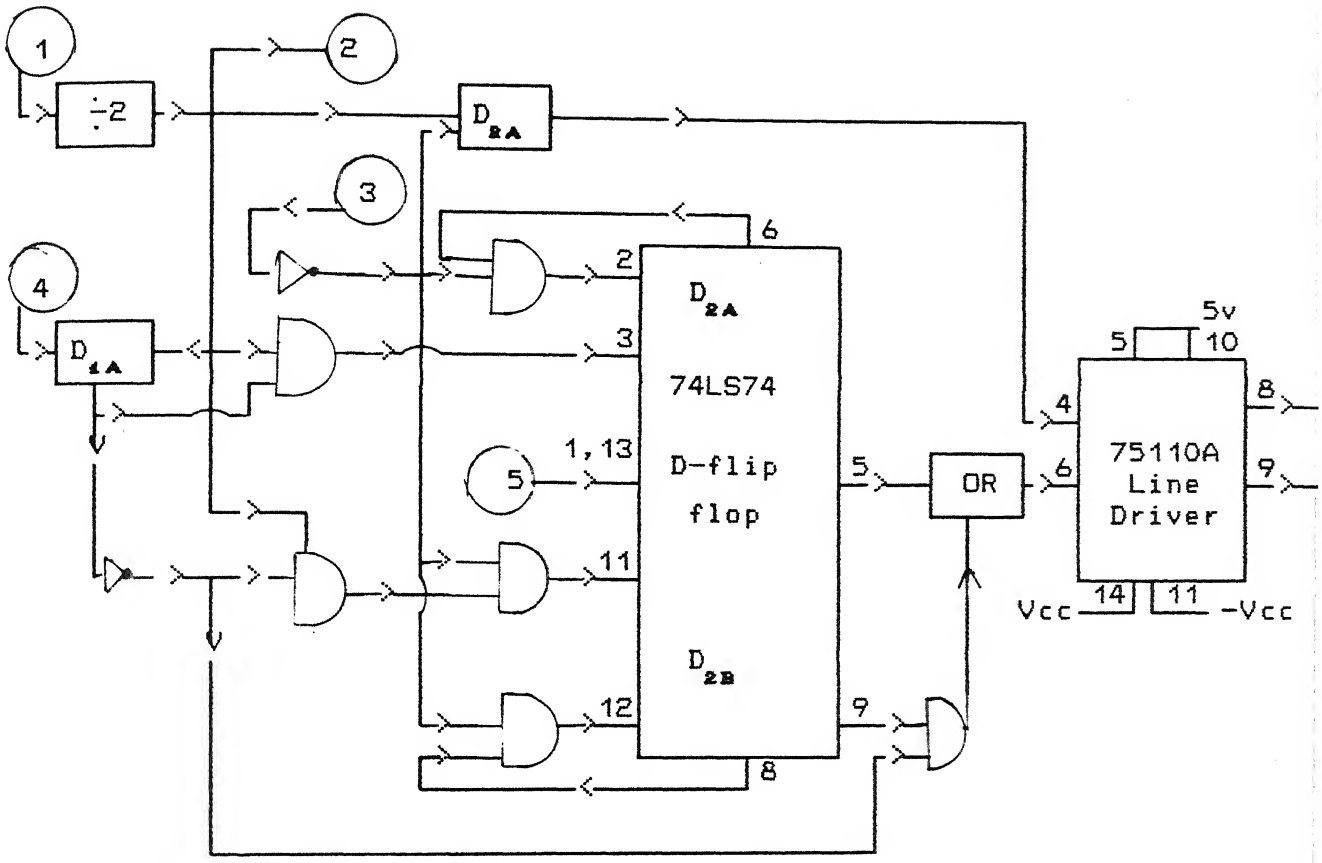
Fig.4.3: Block diagram of the transmitter

SN-75110A, dual line drivers are used to drive the line. The driver circuits feature a constant output current, that is switched to either of the two output terminals by an appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the inhibit inputs. The function table of the line driver is given in Table-1.

Table-4.1: Funtion table of the line driver SN75110A

	Logic inputs		Inhibitor inputs		Outputs	
Pin —> Ser no	A	B	C	D	Y	Z
1	X	X	L	X	OFF	OFF
2	X	X	X	L	OFF	OFF
3	L	X	H	H	ON	OFF
4	X	L	H	H	ON	OFF
5	H	H	H	H	OFF	ON

H-high level, L-low level, X-irrelevant.



(1)- 384 kHz clock from a pulse generator,

(2)- 192 kHz clock to the Data source,

(3)- Data input from the Data source,

(4)- 2/46 pulse from the Data source,

(5)- Frame sync pulse from the Data source.

Vcc - 5V; Pins not used are not shown.

D_{1A},D_{1B} and D_{2A},D_{2B}: Set of two D-flip flops on one chip 74LS74

Fig.4.4: Block schematic of the transmitter

Serial 4 and 5, of the above function table, are the ones which are of interest for the transmission of the data in our set up. The two ORed Q outputs of the D-flip flop, D_2, are fed to one of the line driver inputs, pin 6. Inverted data is fed to the D-input of the D-flip flop (D_{1B}), which is clocked with a 192 kHz clock. The Q output of this D-flip flop is given to the second input of the line driver, (the inhibit input) 75110A. The output at the pins 8 and 9 of the line driver give two bit streams as shown against outputs Y and Z of serial 4 and 5 in the function table. Briefly they are described: to zero corresponds a signal which is high in either of the lines and low in the other, and to one a low level signal appears in both the lines. At the output a three level signal i.e. Pseudo-Ternary bit stream is available, conforming to the ISDN standards laid down by the CCITT.

4.4 RECEIVER

The primary function of the receiver is to recover the data/information from the Pseudo-ternary bit stream. Refer to Fig.4.5. The design of the receiver can be conveniently divided into four parts, as mentioned in sec. 4.1. The basis for the design of the receiver is decoding of the two bit streams transmitted by the line transmitter, 75110A, by the line receiver, 75108A. The line receiver gives the two output bit streams: O_+ and O_-; where O_+ indicates output corresponding to zero in data and this bit stream has +ve polarity. O_- indicates zero in data and

this bit stream also has +ve polarity. In case the data is one then neither of these lines have any polarity i.e. none of these bit streams have any line signal. These two waveforms are then instrumental in the recovery of data, clock and frame sync signal. It should be noted that the clock and the frame sync signal are to be derived in the NT to TE direction only, (refer to section 3.7.1). Each of the blocks of the receiver are dealt with in detail in the following paragraphs.

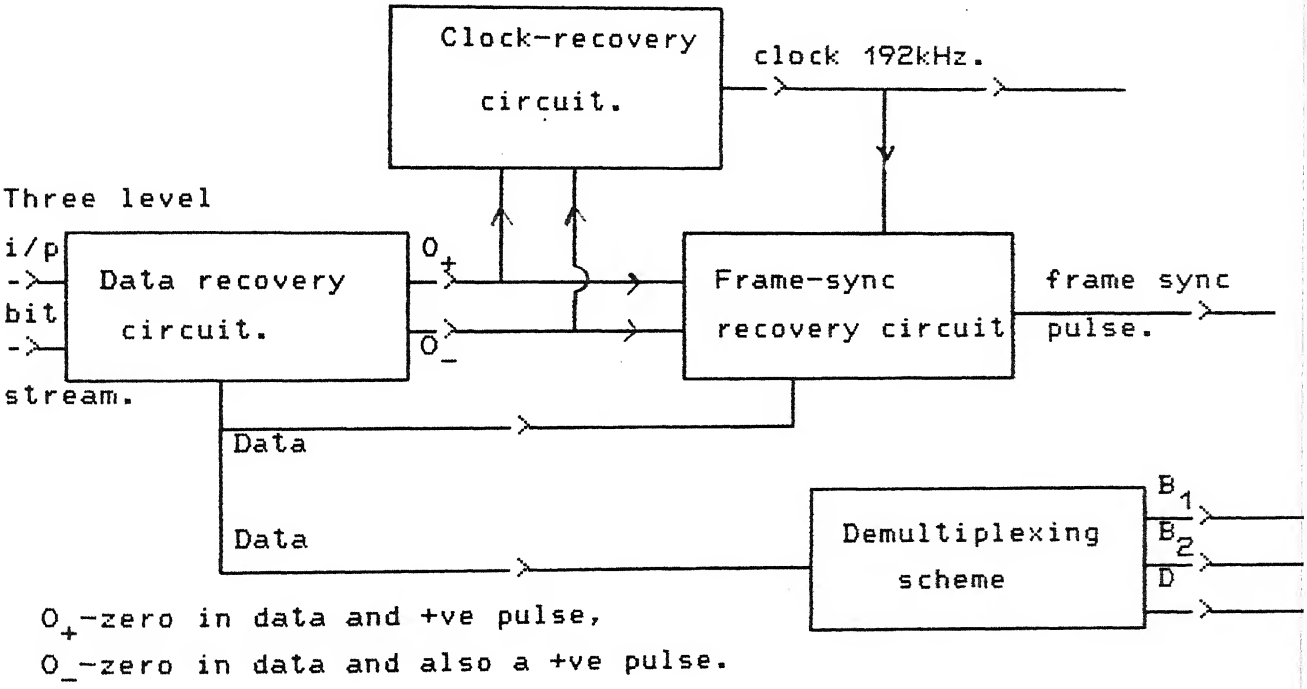
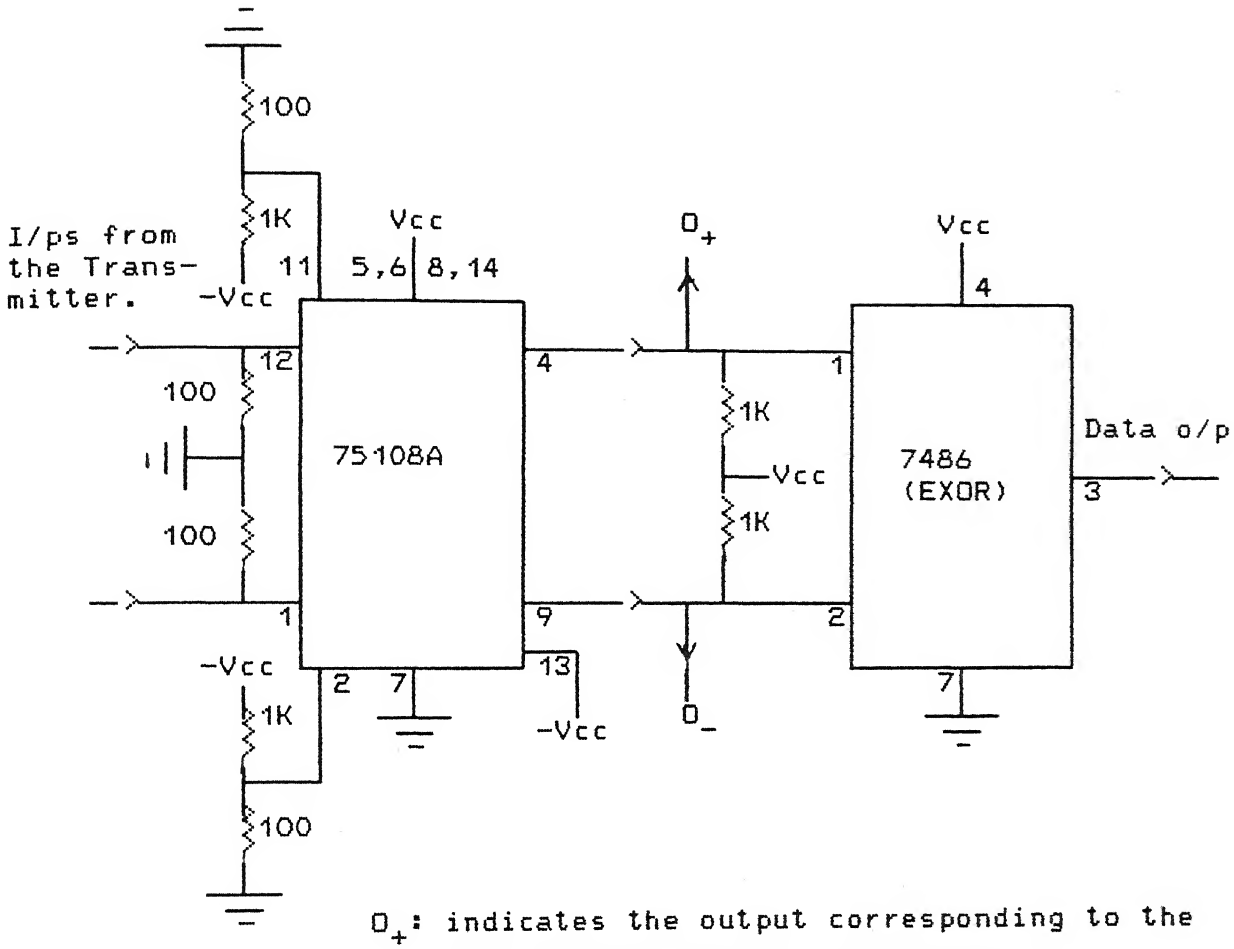


Fig.4.5: Block diagram of the receiver

4.4.1 Data Recovery: The line receiver, 75108A, offers optimum performance when used with line driver, 75110A. 75108A is a high speed line receiver, dual circuit featuring two independent



O_+: indicates the output corresponding to the zero in data and is a +ve pulse.

O_+: indicates the output corresponding to the zero in data, and is also a +ve pulse.

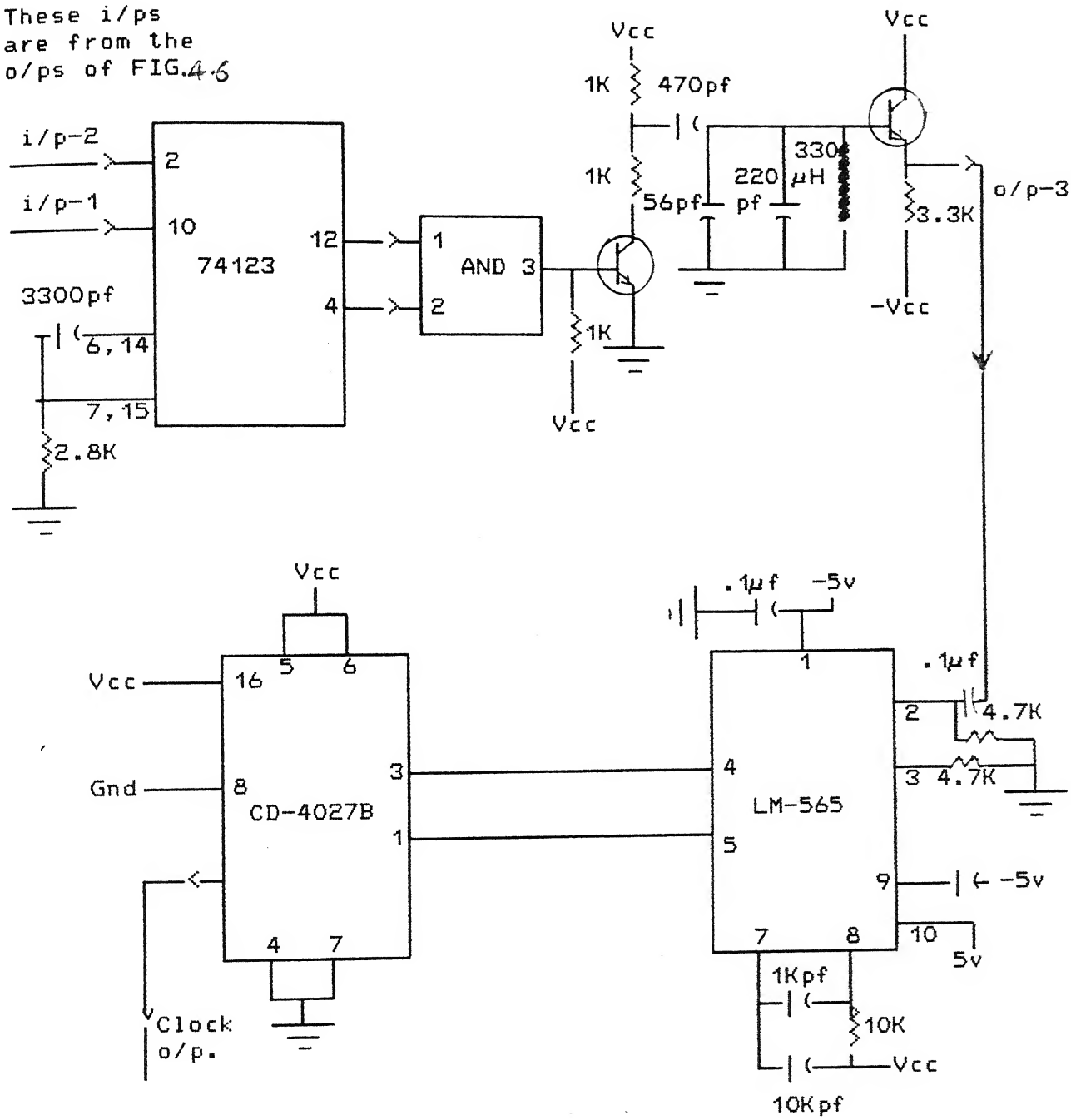
Vcc: 5V.

Pins not used are not shown.

Fig.4.6: Functional diagram for data recovery.

channels. It is designed for general plus specific applications to detect low level signals, in the presence of common mode noise. Thus the choice of the 75108A, as a line receiver. Fig.4.6 gives functional diagram for the recovery of data. The incoming, three level bit stream from the line driver is fed to the two independent inputs (pin 1 and 12) of the line receiver. A voltage divider circuit is connected to the corresponding differential inputs (pins 2 and 11) of the receiver. The outputs of the receiver are available at the pins 4 and 9. These outputs are pulled up by connecting a set of pull up resistors, as 75108A features a open collector output configuration. The resistances have a value of 1kΩ. The two outputs are then fed to an EXor gate, 7486, which gives the requisite data.

4.4.2 Clock recovery. Retriggerable monostable multivibrator, band pass filter, emitter follower and LM-565 (PLL chip) alongwith CD-4027B when connected in series results in the recovery of a synchronised 192 kHz clock. Functional diagram of the clock recovery circuit is given in Fig.4.7. A DC triggered monostable multivibratoer, 74LS123, with a feature of pulse deviation control by selection of external resistances and capacitance value is found suitable for this set up. It is provided with enough schmitt hysteresis to ensure jitter free triggering. The two outputs from the line driver are fed to the input pins, 2 and 10 of the monostable. The outputs of the monostable, from pin 12 and 4 are ANDed and fed to the tuned circuit, tuned at 192 kHz. The tuned



Vcc: 5V.

Pins not used are not shown.

Fig.4.7: Functional diagram for clock recovery

circuit is coupled to a transistor (amplifier) with a 470 μf capacitance. The tuned circuit is a normal L C circuit, having an inductance value of 330 μH and a capacitance value of 220pf in parallel with 56pf. The tuned circuit is coupled to the PLL through an emitter follower. The LM-565 along with CD-4027B results in a synchronised clock of 192 kHz.

4.4.3 Frame sync recovery. The function of this section is to describe the recovery of the frame sync signal from the incoming bit stream. Robust and a general purpose frame sync rcovery cicuit was designed. Realising the frame sync circuit turned out to be most difficult and took considerable amount of time and effort before it could be implemented. At the face of it, it did not seem very difficult, but it was after a great deal of brain storming exercise that the idea of the logic pertaining to the frame sync recovery was conceived.

The scheme is built around the principles of Coincidence, Decision and Cycle Swallowing. Philosophy of the three principles is explained briefly.

a) Coincidence is the act or condition occuring at the same place in space or time. The occurence of the bit positions of various bit streams happen at the same time and seem to have some connection also. This reflects on the decision making circuits results.

b) Decision circuit obtains a solution or a conclusion is arrived at, after considering the results of the coincidence

logic circuit. Its output decides if the cycle swallowing would take place or not.

c) Cycle Swallowing. As the name suggests is a circuit that would swallow a clock cycle depending upon the decision making cicuits output. Physically this results in the counter counting 47 or 48 clocks before giving out the RCO pulse.

Referring to Fig.4.8 and 4.9 it can be seen that at this stage the available bit streams are

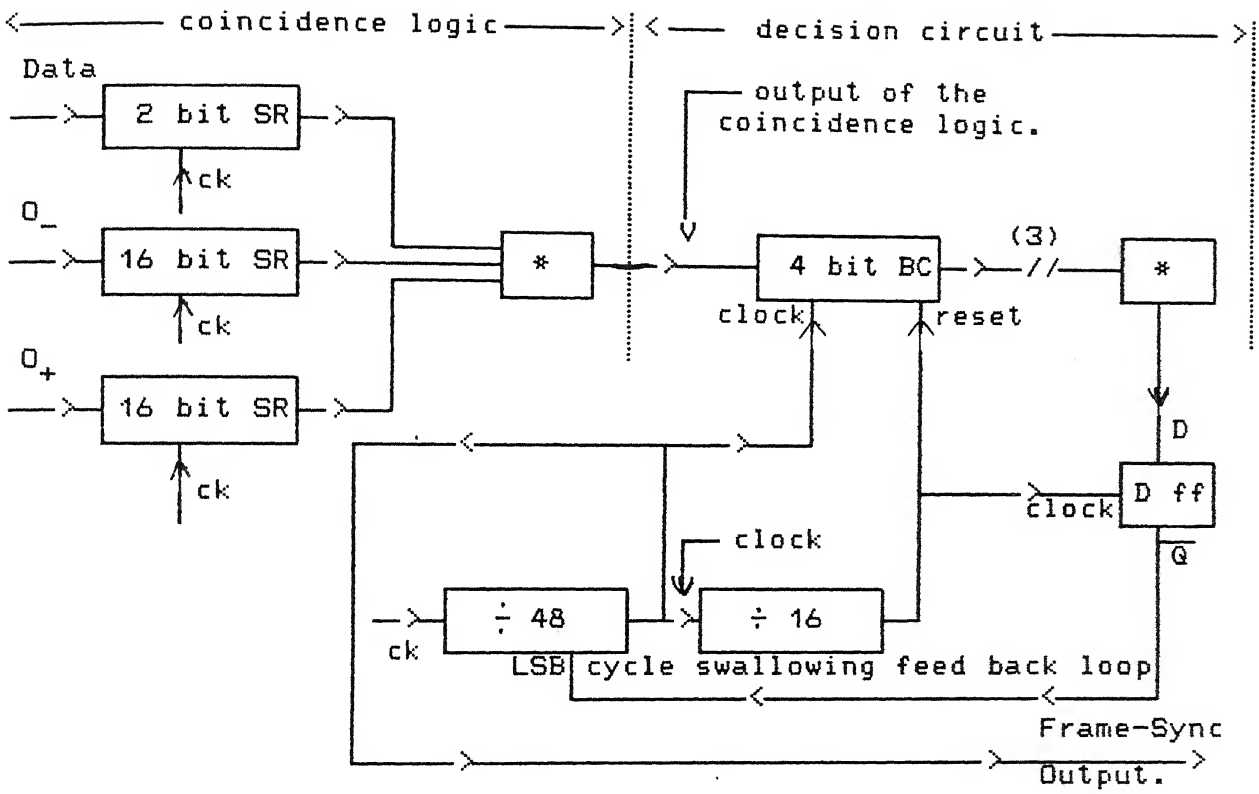
a) data,

b) clock,

c) +ve zero and

d) -ve zero.

As mentioned in sec. 3.7.1, the frame sync is to be acheived in the NT to TE direction; and can be detected at not earlier than 15^{th} bit. Framing is acheived with the help of the framing bit F, its balance bit L, auxiliary framing bit F_A and N ($=\overline{F_A}$). The coincidence logic is a condition, which, when decoded, gives the frame sync signal. Referring to the Fig.3.6, it can be seen that the condition as described occurs only once in a frame; i.e. when F (the framing bit) 1^{st} bit is a zero bit and has a positive polarity, L (the corresponding balance bit) is a zero bit data and has a negative polarity, F_A (Auxiliary framing bit) is again a zero bit but could have either positive or negative polarity, and N ($=\overline{F_A}$) is a one bit and has no polarity. Thus if we delay the F bit by a time period equal to 14 bit period, L bit by 13 bit



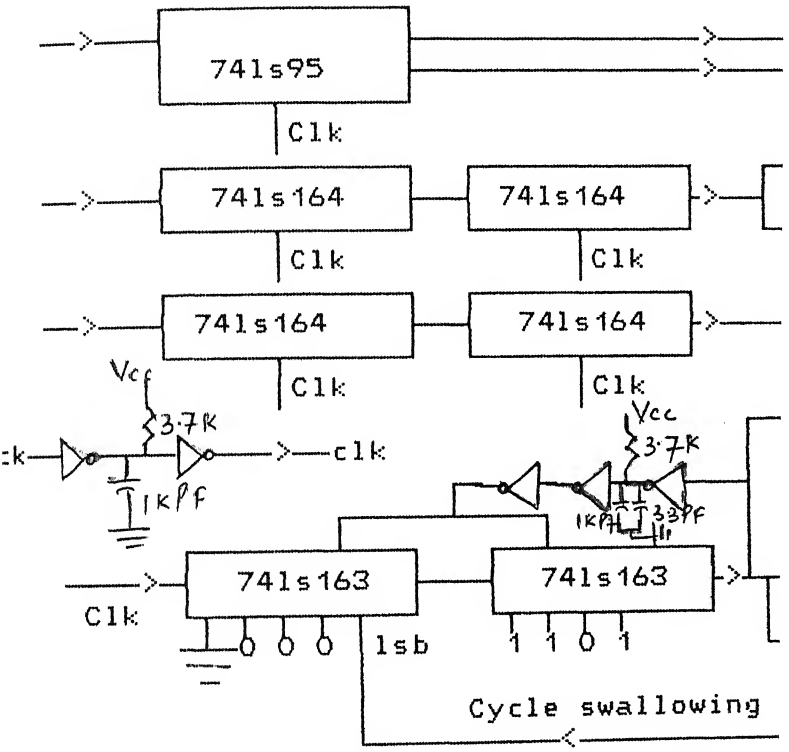
ck- clock input, * - and gate.

O_+- data is zero and has +ve pulse, D ff - D-flip flop,

O_-- data is zero and also has a +ve pulse.

SR - Shift register, BC - binary counter.

Fig.4.8: Block diagram of frame sync recovery



ck - input clock of 192 kHz, clk

Fig.4.9:B1

BC_1 counter output is <14 , the AND gate, 74LS11, output is low,

period and F_A by 1 bit period, and then all these bits along with N bit are ANDed, it would result in a pulse that would be high only when then above condition is met, the pulse would thus correspond to a frame sync signal. But false frame sync pulse could be indicated, if a data having the same sequence/format as the above four bits is received. And a frame sync failure would occur if the noise in the channel distorts any of the four crucial bits. To overcome the above two conditions of frame sync failure or frame sync false triggering, upto a great extent, Cycle-Swallowing technique is resorted to. The output of the And gate is fed to the ENP/ENT inputs of the binary counter (BC_1). Two binary counters, BC_1 and BC_2, are connected in series, in the same configuration as the ones used in Data source, to give a divide by 48 clock pulse; this output is fed to the clock input of the first binary counter (BC_1). The counter BC_1 is made to count for 16 clock cycles and the outputs Q_B, Q_C and Q_D of BC_1 are fed to a three input AND gate, 74LS11. A high at the output of the and gate indicates if the counter has a count >= 14 and a low indicates the count as <14. The output of the AND gate is fed to the D input of a D-flip flop. The $\overline{Q}$ output of the D-flip flop is fed to the LSB of the two binary counters (BC_2 and BC_3), which are connected in series. If the count of the BC_1 is >=14, then the output of the 74LS11 is high thus the D-flip flop is triggered and the output Q is high & $\overline{Q}$ is low. Thus with the output of the And gate as high, the two counters, BC_2 and BC_3, continue to divide by 48. If the BC_1 counter output is <14 , the AND gate, 74LS11, output is low,

thus the D-flip flop is not triggered and the output Q remains low and $\overline{Q}$ is high, i.e. the LSB of the BC_2 counter is high, the two counters now count 47, as against the previous condition where they counted upto 48. Thus a Cycle Swallowing is said to have taken place. Another binary counter, BC_4, clocked by the RCO output of the BC_3, gives a pulse after 16 frames, this pulse resets the counter BC_1. This ensures that cycle swallowing takes place only in one frame in a set of 16 frames. The counters, BC_2 and BC_3, will there after continue to give a pulse once after every 48 bits, so long as the count value of the counter, BC_1, is >=14. In case the count value of the BC_1 counter is <14, cycle swallowing will take place once every 16 frames and would continue to do so till the condition of the coincidence circuit is met. The frame sync pulse has a time period delay of equivalent of 15 bits time period from the frame sync being generated at the Data Source. This has to be kept in mind while implementing the demultiplexing scheme.

Maximum time taken for the frame sync can be calculated as follows:

a) Time duration of each pulse =5.2 μ secs.

b) Time duration for a frame (48 bits) =48 * 5.2 μ secs
= 250 μ secs.

c) Time duration for a frame with a cycle swallow (47 bits) =47 * 5.2 μsecs
=245 μ secs.

d) Maximum time taken for the frame sync to take place is calculated as under:

When the system is switched on, the worst case would be that the first bit received at the receiver is the third bit in a frame i.e. first information bit after the balance bit corresponding to the framing bit. Thus the maximum time is

$$= \left[(47 + 48*15) * 46 + 48 * 16 \right] * 5.2\ \mu \text{ secs.}$$

$$= 187 \text{ m secs.}$$

e) The average delay is calculated as

$$= \left[(47 + 48 * 15) * 23 + 48 * 16 \right] * 5.2\ \mu \text{ secs}$$

$$= 95 \text{ m secs.}$$

The maximum and average delay time period lay down the conditions for starting the data transmission after the system is switched on. It is seen that in the worst case the delay is less than 2 m.s. which is not asking for too much, as it takes over a sec to withdraw ones hand after switching on a PC.

Frame sync failure would take place if the channel is so noisy that the crucial four bits get distorted three or more times out of sixteen frames OR if the data has the same format for fifteen or sixteen times out of sixteen frames.

4.5 SUMMARY

At the time of submission of the Thesis the status of the project is as under:

a) Random data i.e. B_1, B_2 and D which is made available at

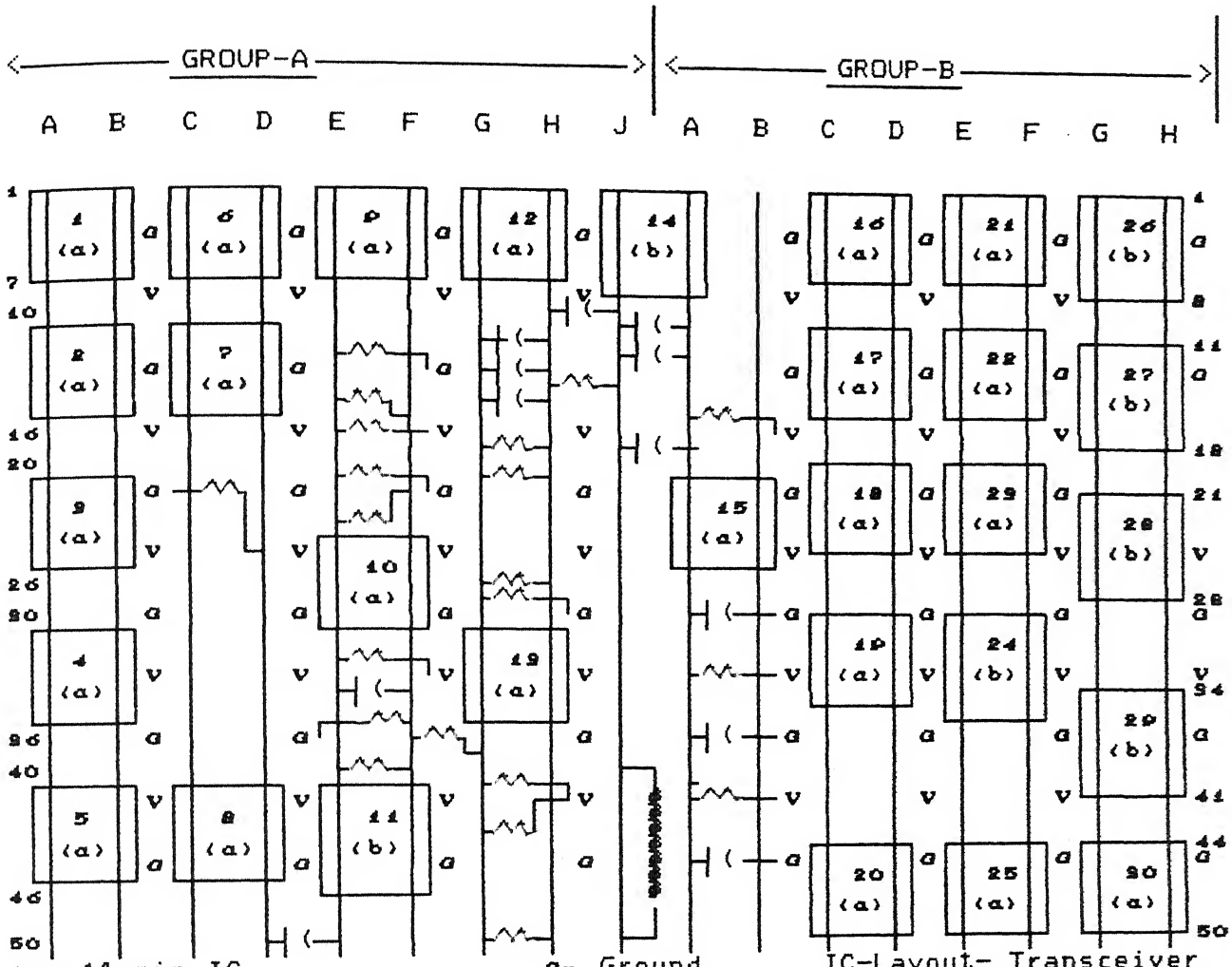
the parallel inputs of the shift registers, alongwith the requisite code bits are generated by the Data source at 192 kbs rate, and are fed to the Pseudo-Ternary Transmitter.

b) The three level code corresponding to the data generated by the Data source is available at the two output terminals of the transmitter.

c) In the receiver the data recovery circuit recovers the original data from the Pseudo-Ternary bit stream.

d) Clock, syncronised with the inputy clock, is also recovered from the Psuedo-Ternary bit stream.

e) Frame sync pulse with the delay of 15 bits from the input frame sync pulse is obtained by the frame sync recovery circuit.



(a)-14 pin IC.

(b)-16 pin IC.

g- Ground,

v- Vcc.

IC-Layout- Transceiver

FIG-4.10

Details of IC's used-

ser. no.	name of ic
1	74ls74
2	74ls74
3	7408
4	7404
5	7408
6	74ls74
7	75110A
8	7432
9	7486
10	75108A
11	74123
12	LM-565
13	7403
14	CD-4027
15	74ls14

ser. no.	name of ic.
16	74ls04
17	74ls164
18	74ls164
19	7421
20	74ls74
21	74ls164
22	74ls164
23	74ls95
24	74ls163
25	74ls74
26	74ls163
27	74ls163
28	74ls163
29	7408
30	74ls11

PIN CONNECTIONS

IC.NO. 1 (741s74)

Pin No.	From	To
1	A/1	A/10
2	A/2	A/6
3	A/3	A/33
4	A/4	Vcc
5	A/5	C/3,A/21
6	A/6	A/2
7	A/7	Gnd
8	B/7	B/3
9	B/6	Clock (192 kbs)
10	B/5	Vcc
11	B/4	A/32
12	B/3	B/7
13	B/2	NC
14	B/1	Vcc

IC.NO. 2 (741s74)

Pin No.	From	To
1	A/10	A/1,B/11
2	A/11	B/23
3	A/12	A/22
4	A/13	Vcc
5	A/14	D/41
6	A/15	B/21
7	A/16	Gnd
8	B/16	B/24
9	B/15	A/43
10	B/14	Vcc
11	B/13	B/46
12	B/12	B/26
13	B/11	A/10
14	B/10	Vcc

IC NO. 3 (7408)

1	A/20	A/30
2	A/21	A/5,A/24
3	A/22	A/12
4	A/23	A/31
5	A/24	A/21
6	A/25	B/45
7	A/26	Gnd
8	B/26	B/12
9	B/25	B/32
10	B/24	B/16
11	B/23	A/11
12	B/22	B/32,B/44
13	B/21	A/15

IC NO. 4 (7404)

1	A/30	A/20,A/6
2	A/31	A/23,A/41
3	A/32	B/4,I/P
4	A/33	A/3
5	A/34	NC
6	A/35	NC
7	A/36	Gnd
8	B/36	NC
9	B/35	NC
10	B/34	NC
11	B/33	NC
12	B/32	B/22,B/25 C/2
13	B/31	I/P(DATA)

14	B/20	Vcc	14	B/30	Vcc

IC NO. 5 (7408)

1	A/40	NC
2	A/41	NC
3	A/42	NC
4	A/43	B/15
5	A/44	A/31
6	A/45	D/42
7	A/46	Gnd
8	B/46	B/13
9	B/45	A/25
10	B/44	B/32
11	B/43	NC
12	B/42	NC
13	B/41	NC
14	B/40	Vcc

IC NO. 6 (741s74)

1	C/1	NC
2	C/2	B/33
3	C/3	A/5,D/3
4	C/4	Vcc
5	C/5	C/15
6	C/6	NC
7	C/7	Gnd
8	D/7	NC
9	D/6	A/20,A/30
10	D/5	Vcc
11	D/4	C/3
12	D/3	I/P
13	D/2	NC
14	D/1	Vcc

IC NO. 7 (75110A)

1	C/12	NC
2	C/13	NC.
3	C/14	NC
4	C/15	C/5
5	C/16	Vcc
6	C/17	D/43
7	C/18	Gnd
8	D/18	F/26
9	D/17	E/24
10	D/16	Vcc
11	D/15	-Vcc,F/25
12	D/14	NC
13	D/13	NC
14	D/12	Vcc

IC NO. 8 (7432)

1	C/40	NC
2	C/41	NC
3	C/42	NC
4	C/43	NC
5	C/44	NC
6	C/45	NC
7	C/46	Gnd
8	D/46	NC
9	D/45	NC
10	D/44	NC
11	D/43	C/17
12	D/42	A/45
13	D/41	A/14
14	D/40	Vcc

IC NO.9 (7486)

1	E/1	F/29,E/41
2	E/2	E/27,F/46
3	E/3	D/6(gp 2)
4	E/4	NC
5	E/5	NC
6	E/6	NC
7	E/7	Gnd
8	F/7	NC
9	F/6	NC
10	F/5	NC
11	F/4	NC
12	F/3	NC
13	F/2	NC
14	F/1	Vcc

IC NO. 10 (75108A)

1	E/24	D/17,E/20
2	E/25	E/15,E/17
3	E/26	NC
4	E/27	E/2,E/17
5	E/28	C/1(gp 2) Vcc
6	E/29	Vcc
7	E/30	Gnd
8	F/30	Vcc
9	F/29	E/1,E/32
10	F/28	NC
11	F/27	F/36,F/21
12	F/26	D/18,D/25
13	F/25	D/15,F/16
14	F/24	Vcc

IC NO. 11 (74123)

1	E/40	Gnd
2	E/41	E/1
3	E/42	Vcc
4	E/43	G/30
5	E/44	NC
6	E/45	E/50
7	E/46	F/39
8	E/47	Gnd
9	F/47	Gnd
10	F/46	E/2
11	F/45	Vcc
12	F/44	G/31
13	F/43	NC
14	F/42	E/34
15	F/41	F/34,F/37
16	F/40	Vcc

IC NO.12 (LM-565)

1	G/1	F/15
2	G/2	G/28,J/9
3	G/3	H/14
4	G/4	J/3
5	G/5	J/1
6	G/6	NC
7	G/7	A/10,A/12
8	H/7	J/10,A/16
9	H/6	J/18
10	H/5	Vcc
11	H/4	NC
12	H/3	NC
13	H/2	NC
14	H/1	NC

IC NO.13 (7403)

1	G/30	E/43
2	G/31	F/44
3	G/32	G/27,H/24
4	G/33	NC
5	G/34	NC
6	G/35	NC
7	G/36	Gnd
8	H/36	NC
9	H/35	NC
10	H/34	NC
11	H/33	NC
12	H/32	NC
13	H/31	NC
14	H/30	Vcc

IC NO. 14 (CD 4027)

1	J/1	G/5
2	J/2	B/23(gp2)
3	J/3	G/4 Clock.
4	J/4	Gnd
5	J/5	Vcc
6	J/6	Vcc
7	J/7	Gnd
8	J/8	Gnd
9	A/8 (gp 2)	NC
10	A/7 "	NC
11	A/6 "	NC
12	A/5 "	NC
13	A/4 "	NC
14	A/3 "	NC
15	A/2 "	NC
16	A/1 "	Vcc

IC NO 15 (741s14)

1	A/20	G/45
2	A/21	E/29
3	A/22	H/25
4	A/23	A/24
5	A/24	A/23,A/36,A/40
6	A/25	B/25 A/44
7	A/26	Gnd
8	B/26	H/18
9	B/25	A/25
10	B/24	F/24,A/28,B/21
11	B/23	J/2
12	B/22	D/16
13	B/21	B/24,A/32,
14	B/20	Vcc

IC NO 16 (741s08)

1	C/1	E/27
2	C/2	C/11
3	C/3	NC
4	C/4	NC
5	C/5	C/45
6	C/6	G/44
7	C/7	Gnd
8	D/7	E/19,Data
9	D/6	E/3
10	D/5	D/33
11	D/4	F/21
12	D/3	E/2
13	D/2	F/29
14	D/1	Vcc

IC NO 17 (74ls164)

1	C/10	Vcc
2	C/11	C/2
3	C/12	NC
4	C/13	NC
5	C/14	NC
6	C/15	NC
7	C/16	Gnd
8	D/16	D/25,B/22,E/46
9	D/15	Vcc
10	D/14	NC
11	D/13	NC
12	D/12	NC
13	D/11	C/20
14	D/10	Vcc

IC NO 18 (74ls164)

1	C/19	Vcc
2	C/20	D/11
3	C/21	NC
4	C/22	NC
5	C/23	NC
6	C/24	NC
7	C/25	Gnd
8	D/25	D/16,F/7
9	D/24	Vcc
10	D/23	NC
11	D/22	NC
12	D/21	D/30
13	D/20	NC
14	D/19	Vcc

IC NO 19 (7421)

1	C/29	NC
2	C/30	NC
3	C/31	NC
4	C/32	NC
5	C/33	NC
6	C/34	NC
7	C/35	Gnd
8	D/35	E/35
9	D/34	F/20
10	D/33	D/5
11	D/32	NC
12	D/31	F/13
13	D/30	D/21
14	D/29	Vcc

IC NO 20 (74ls74)

1	C/44	Vcc
2	C/45	C/5,H/50
3	C/46	G/46
4	C/47	H/46
5	C/48	NC
6	C/49	G/3
7	C/50	Gnd
8	D/50	NC
9	D/49	NC
10	D/48	NC
11	D/47	NC
12	D/46	NC
13	D/45	NC
14	D/44	Vcc

IC NO 21 (74ls164)

1	E/1	Vcc
2	E/2	D/3
3	E/3	NC
4	E/4	NC

IC NO 22 (74ls164)

1	E/10	Vcc
2	E/11	F/2
3	E/12	NC
4	E/13	NC

5	E/5	NC	5	E/14	NC
6	E/6	NC	6	E/15	NC
7	E/7	Gnd	7	E/16	Gnd
8	F/7	G/2,D/25,F/16	8	F/16	F/7
9	F/6	Vcc	9	F/15	Vcc
10	F/5	NC	10	F/14	NC
11	F/4	NC	11	F/13	D/31
12	F/3	NC	12	F/12	NC
13	F/2	E/11	13	F/11	NC
14	F/1	Vcc	14	F/10	Vcc

IC NO 23 (74ls95)

1	E/19	D/7
2	E/20	NC
3	E/21	NC
4	E/22	NC
5	E/23	NC
6	E/24	Gnd
7	E/25	Gnd
8	F/25	NC
9	F/24	B/24
10	F/23	NC
11	F/22	NC
12	F/21	D/4
13	F/20	D/34
14	F/19	Vcc

IC NO 24 (74ls163)

1	E/29	A/21
2	E/30	H/12,E/45
3	E/31	NC
4	E/32	NC
5	E/33	NC
6	E/34	NC
7	E/35	D/35,F/35
8	E/36	Gnd
9	F/36	Vcc
10	F/35	E/35
11	F/34	H/49
12	F/33	H/48
13	F/32	H/47
14	F/31	NC
15	F/30	NC
16	F/29	Vcc

IC NO 25 (74s74)

1	E/44	Vcc
2	E/45	E/30,H/12
3	E/46	D/25,F/47
4	E/47	Vcc
5	E/48	F/46
6	E/49	NC
7	E/50	Gnd

IC NO 26 (74ls163)

1	G/1	Vcc
2	G/2	F/7,G/12
3	G/3	C/49
4	G/4	Gnd
5	G/5	Gnd
6	G/6	Gnd
7	G/7	Vcc

8	F/50	NC
9	F/49	Fr. Sync.
10	F/48	Vcc
11	F/47	E/46
12	F/46	E/48
13	F/45	Vcc
14	F/44	Vcc

8	G/8	Gnd
9	H/8	H/18
10	H/7	Vcc
11	H/6	NC
12	H/5	NC
13	H/4	NC
14	H/3	NC
15	H/2	H/17
16	H/1	Vcc

IC NO 27 (74ls163)

1	G/11	Vcc
2	G/12	G/2
3	G/13	Vcc
4	G/14	Gnd
5	G/15	Vcc
6	G/16	Vcc
7	G/17	H/17
8	G/18	Gnd
9	H/18	B/26,H/8
10	H/17	G/17,H/2
11	H/16	NC
12	H/15	NC
13	H/14	NC
14	H/13	NC
15	H/12	E/45,G/22
16	H/11	Vcc

IC NO 28 (74ls163)

1	G/21	Vcc
2	G/22	H/12,H/45
3	G/23	NC
4	G/24	NC
5	G/25	NC
6	G/26	NC
7	G/27	Vcc
8	G/28	Gnd
9	H/28	Vcc
10	H/27	Vcc
11	H/26	NC
12	H/25	NC
13	H/24	NC
14	H/23	NC
15	H/22	H/36,G/45
16	H/21	Vcc

IC NO 29 (7408)

1	G/34	Vcc
2	G/35	G/39
3	G/36	C/46
4	G/37	Vcc
5	G/38	H/40
6	G/39	G/35
7	G/40	Gnd
8	H/40	G/38

IC NO 30 (74ls11)

1	G/44	C/6
2	G/45	H/22,A/20
3	G/46	NC
4	G/47	NC
5	G/48	NC
6	G/49	NC
7	G/50	Gnd
8	H/50	C/45

9	H/39	H/37	9	H/49	F/34
10	H/38	Vcc	10	H/48	F/33
11	H/37	H/39	11	H/47	F/32
12	H/36	H/22	12	H/46	C/47
13	H/35	Vcc	13	H/45	A/22,G/22
14	H/34	Vcc	14	H/44	Vcc

CHAPTER-5

CONCLUSION

Conclusion is an inappropriate word here, as this is just the begining for the author where he has just had a cursory look at the SUPERNETWORK - THE ISDN. Undoubtly this project has been a mile stone in understanding the directions of ISDN.

5.1 ACHEIVEMENTS

Though the implementation of the transceiver is a small part of a sub-system and may seem trivial,the major acheivement has been the scheme for frame synchronisation. The scheme is a fairly general and robust one. Delay lock loop implementation along with suitable changes in the cycle swallowing feed back loop (according to the application),permit it to be used in a variety of link applications; such as error correcting codes etc. The fabricated transceiver has been tested over a period of time along with the data source/frame simulator and it has performed satisfactorily.

5.2 SHORTCOMINGS

Pity that for want of an IC and paucity of time, a working link was not shown. Non availabilty of the CODEC

IC's-HD44235, HD44236, HD44237 and HD44238 lead to the truncation of the thesis at a stage where a working link could not be shown. The main difference between the available CODEC chip and the above mentioned chips is that HD44235-..38 can accept any clock from 64kHz to 2.048MHz, whereas the available ones accept only one of 1.536MHz, 1.544MHz or 2.048MHz clock. However, the main idea of acheiving a three level signal from a binary data and recovery backof the data, clock and frame sync has been implemented. A block diagram as regards the multiplexing in the transmitter is shown in Fig.5.1.

5.3 FUTURE USEFULNESS

Besides understanding the CCITT recommendations on ISDN, the aim of this experiment was to fabricate,in MSI chip configuration, the ISDN basic access pseudo-ternary transceiver. Timing recovery circuit and frame sync recovery circuit formed major part of it. The fabrication upto a great extent succeeded in reducing the chip configuration level to that of flip-flops and gates. It is thus visualised that the same could now be implemented on Programmable logic arrays (PLA's) or Field programmable gate arrays (FPGA's) for the ISDN interface. One of the available LSI chip technology interface configuration is built around IC-29C53 Transceiver.

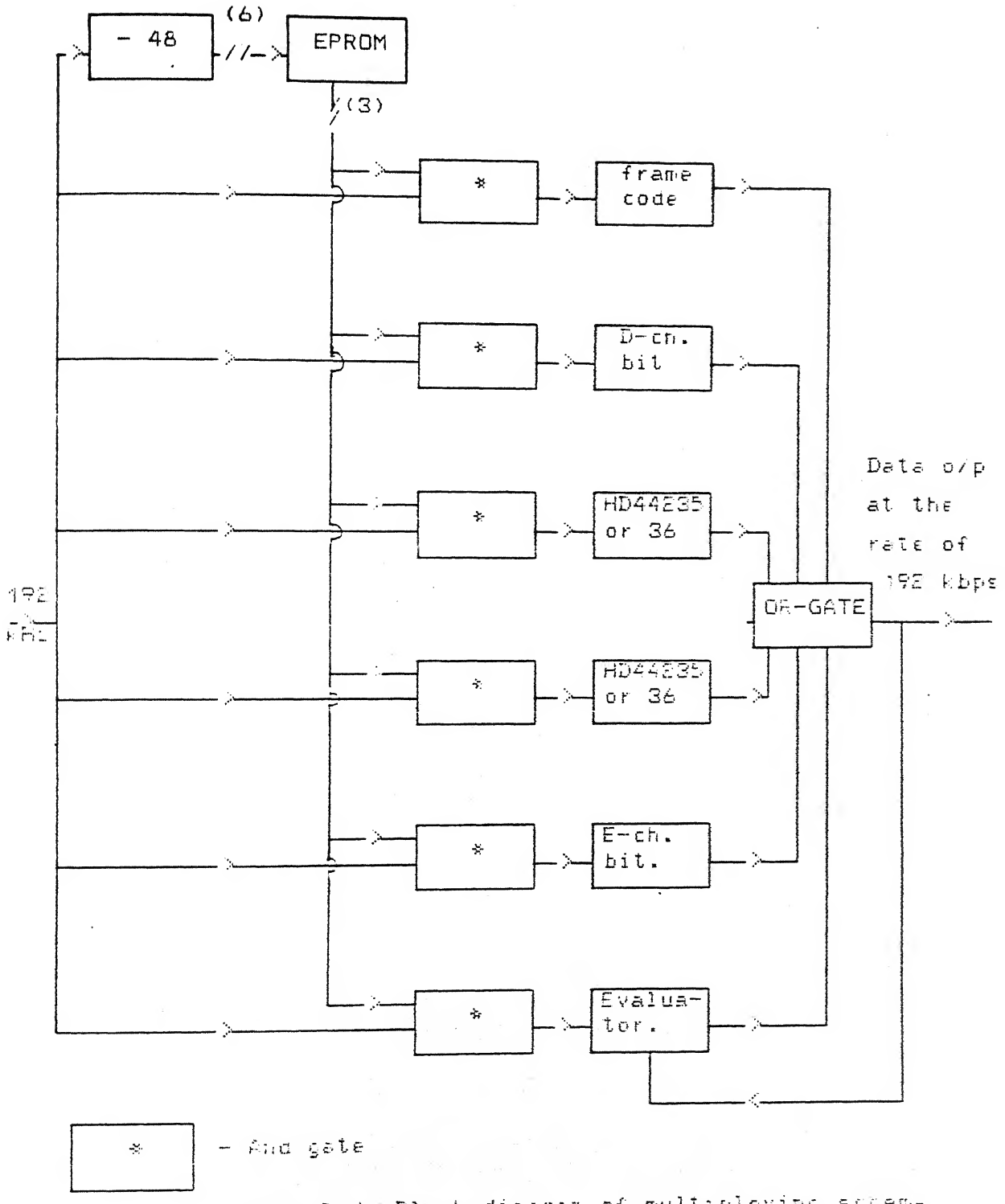


Fig.5.1: Block diagram of multiplexing scheme

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